



CEP12N5/CEB12N5

CEF12N5

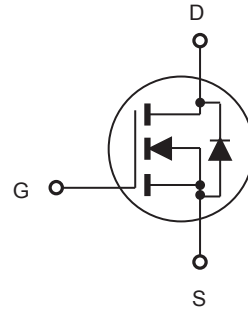
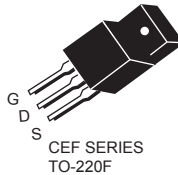
N-Channel Enhancement Mode Field Effect Transistor

PRELIMINARY

FEATURES

Type	V _{DSS}	R _{DS(ON)}	I _D	@V _{GS}
CEP12N5	500V	0.54Ω	12A	10V
CEB12N5	500V	0.54Ω	12A	10V
CEF12N5	500V	0.54Ω	12A ^d	10V

- Super high dense cell design for extremely low R_{DS(ON)}.
- High power and current handling capability.
- Lead free product is acquired.



ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V _{DS}	500		V
Gate-Source Voltage	V _{GS}	±30		V
Drain Current-Continuous	I _D	12	12 ^d	A
Drain Current-Pulsed ^a	I _{DM} ^e	48	48 ^d	A
Maximum Power Dissipation @ T _C = 25°C - Derate above 25°C	P _D	166	50	W
		1.3	0.4	W/°C
Operating and Store Temperature Range	T _J , T _{stg}	-55 to 150		°C

Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R _{θJC}	0.75	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	65	°C/W

This is preliminary information on a new product in development now .
Details are subject to change without notice .

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<http://www.cetsemi.com>



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Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	500			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 500V, V_{GS} = 0V$			1	μA
Gate Body Leakage Current, Forward	I_{GSSF}	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	I_{GSSR}	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
On Characteristics ^b						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 6A$		0.45	0.54	Ω
Dynamic Characteristics ^c						
Input Capacitance	C_{iss}	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0\text{ MHz}$		1745		pF
Output Capacitance	C_{oss}			205		pF
Reverse Transfer Capacitance	C_{rss}			20		pF
Switching Characteristics ^c						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250V, I_D = 12A, V_{GS} = 10V, R_{GEN} = 25\Omega$		31.6	63.2	ns
Turn-On Rise Time	t_r			25.6	51.2	ns
Turn-Off Delay Time	$t_{d(off)}$			146.3	292.6	ns
Turn-Off Fall Time	t_f			32	64	ns
Total Gate Charge	Q_g	$V_{DS} = 400V, I_D = 12A, V_{GS} = 10V$		44.1	58.7	nC
Gate-Source Charge	Q_{gs}			7.3		nC
Gate-Drain Charge	Q_{gd}			17.3		nC
Drain-Source Diode Characteristics and Maximum Ratings						
Drain-Source Diode Forward Current	I_S^f				12	A
Drain-Source Diode Forward Voltage ^b	V_{SD}^g	$V_{GS} = 0V, I_S = 12A$			1.4	V
Notes : <input type="checkbox"/> a. Repetitive Rating : Pulse width limited by maximum junction temperature . b. Pulse Test : Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$. <input type="checkbox"/> c. Guaranteed by design, not subject to production testing. <input type="checkbox"/> d. Limited only by maximum temperature allowed . e. Pulse width limited by safe operating area . f. Full package $I_S(max) = 6A$. g. Full package V_{SD} test condition $I_S = 6A$. h. L = 15mH, $I_{AS} = 8.5A, V_{DD} = 50V, R_G = 25\Omega$, Starting $T_J = 25\text{ C}$						



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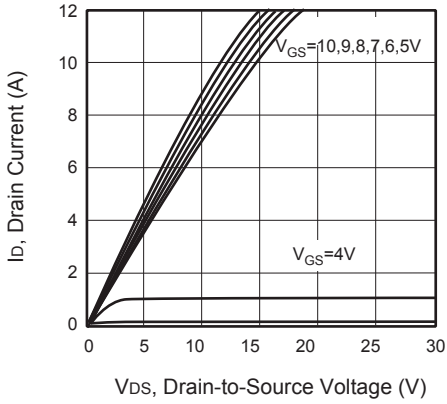


Figure 1. Output Characteristics

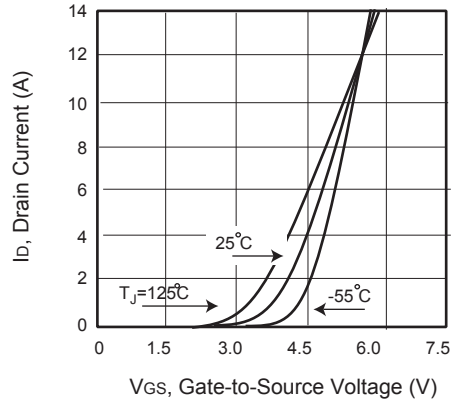


Figure 2. Transfer Characteristics

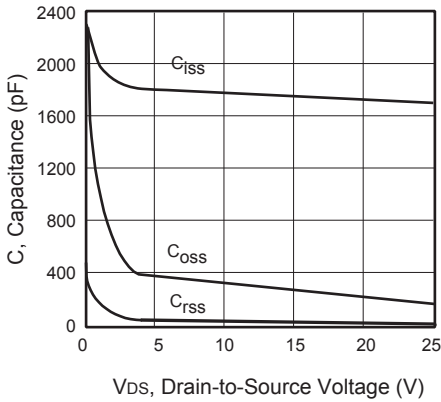


Figure 3. Capacitance

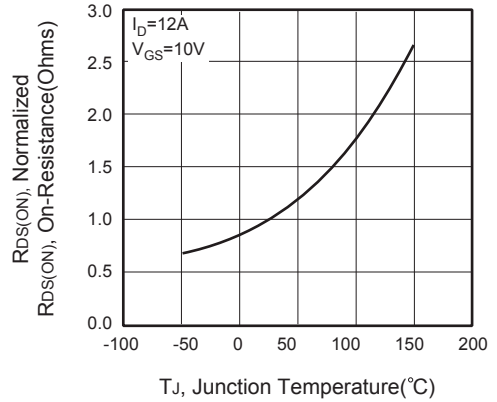


Figure 4. On-Resistance Variation with Temperature



Figure 5. Gate Threshold Variation with Temperature

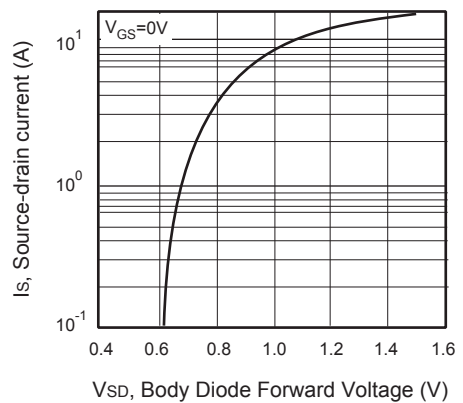


Figure 6. Body Diode Forward Voltage Variation with Source Current



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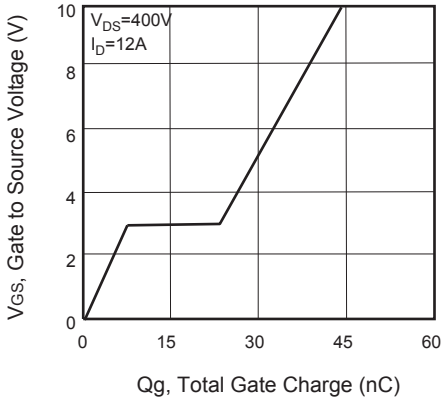


Figure 7. Gate Charge

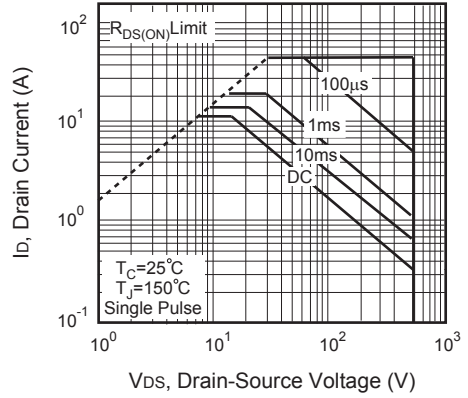


Figure 8. Maximum Safe Operating Area

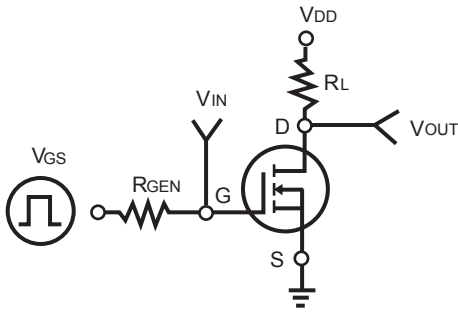


Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

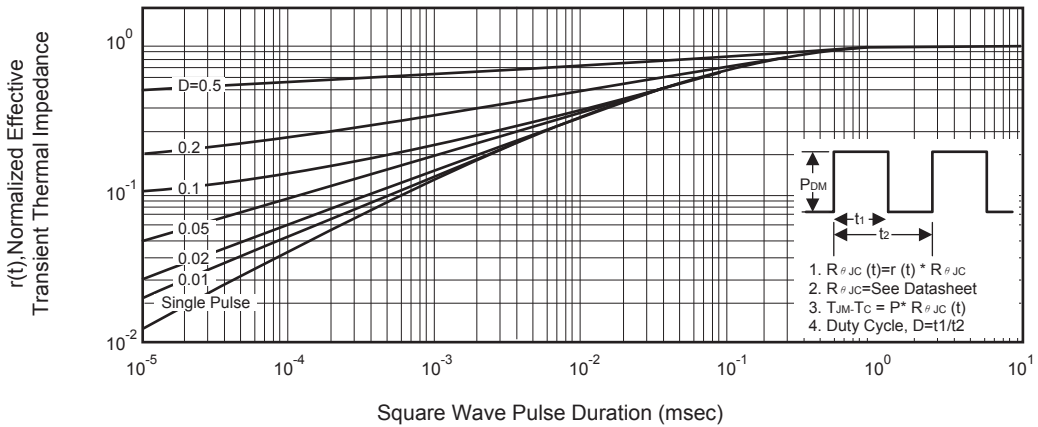


Figure 11. Normalized Thermal Transient Impedance Curve