



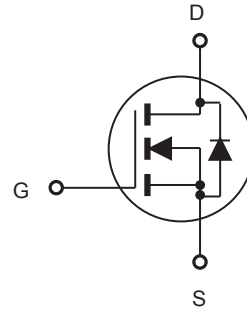
# CEP03N8/CEB03N8 CEF03N8

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

Type	V <sub>DSS</sub>	R <sub>DS(ON)</sub>	I <sub>D</sub>	@V <sub>GS</sub>
CEP03N8	800V	4.8Ω	3A	10V
CEB03N8	800V	4.8Ω	3A	10V
CEF03N8	800V	4.8Ω	3A <sup>d</sup>	10V

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- Lead-free plating ; RoHS compliant.



### ABSOLUTE MAXIMUM RATINGS $T_C = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Limit		Units
		TO-220/263	TO-220F	
Drain-Source Voltage	V <sub>DS</sub>	800		V
Gate-Source Voltage	V <sub>GS</sub>	±30		V
Drain Current-Continuous @ T <sub>C</sub> = 25 °C □ @ T <sub>C</sub> = 100 °C	I <sub>D</sub>	3	3 <sup>d</sup>	A
		2	2 <sup>d</sup>	A
Drain Current-Pulsed <sup>a</sup>	I <sub>DM</sub> <sup>e</sup>	12	12 <sup>d</sup>	A
Maximum Power Dissipation @ T <sub>C</sub> = 25 °C - Derate above 25 °C	P <sub>D</sub>	125	47	W
		0.8	0.3	W/°C
Single Pulsed Avalanche Energy <sup>h</sup>	E <sub>AS</sub>	32		mJ
Single Pulsed Avalanche Current <sup>h</sup>	I <sub>AS</sub>	3		A
Operating and Store Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 175		°C

### Thermal Characteristics

Parameter	Symbol	Limit		Units
Thermal Resistance, Junction-to-Case	R <sub>θJC</sub>	1.2	3.2	°C/W
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	62.5	62.5	°C/W



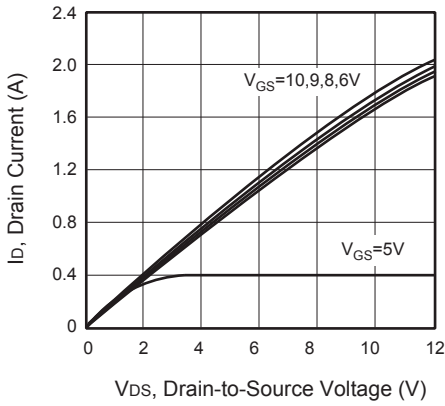
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## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

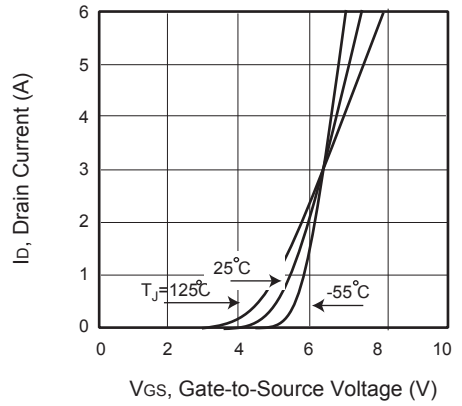
Parameter	Symbol	Test Condition	Min	Typ	Max	Units
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	800			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 800V, V_{GS} = 0V$			1	$\mu A$
Gate Body Leakage Current, Forward	$I_{GSSF}$	$V_{GS} = 30V, V_{DS} = 0V$			100	nA
Gate Body Leakage Current, Reverse	$I_{GSSR}$	$V_{GS} = -30V, V_{DS} = 0V$			-100	nA
<b>On Characteristics<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	2		4	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 1.5A$		3.8	4.8	$\Omega$
Gate input resistance	$R_g$	f=1MHz, open Drain		3.3		$\Omega$
<b>Dynamic Characteristics<sup>c</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0 \text{ MHz}$		690		pF
Output Capacitance	$C_{oss}$			70		pF
Reverse Transfer Capacitance	$C_{rss}$			15		pF
<b>Switching Characteristics<sup>c</sup></b>						
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 450V, I_D = 2.2A,$ $V_{GS} = 10V, R_{GEN} = 25\Omega$		20	40	ns
Turn-On Rise Time	$t_r$			34	68	ns
Turn-Off Delay Time	$t_{d(off)}$			44	88	ns
Turn-Off Fall Time	$t_f$			28	56	ns
Total Gate Charge	$Q_g$	$V_{DS} = 720V, I_D = 2.2A,$ $V_{GS} = 10V$		16	20	nC
Gate-Source Charge	$Q_{gs}$			3		nC
Gate-Drain Charge	$Q_{gd}$			7		nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
Drain-Source Diode Forward Current	$I_S$				3	A
Drain-Source Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$V_{GS} = 0V, I_S = 3A$			1.2	V
Reverse Recovery Time	$T_{rr}$	$I_D = 5A, di/dt = 100A/\mu s$			429	ns
Reverse Recovery Charge	$Q_{rr}$	$I_D = 5A, di/dt = 100A/\mu s$			1.3	nC
<b>Notes :</b> □ a.Repetitive Rating : Pulse width limited by maximum junction temperature . b.Pulse Test : Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 2\%$ . □ c.Guaranteed by design, not subject to production testing. □ d.Limited only by maximum temperature allowed . e.Pulse width limited by safe operating area . □ h.L = 7mH, IAS =3A, VDD = 50V, RG = 25 $\Omega$ , Starting TJ = 25 C						



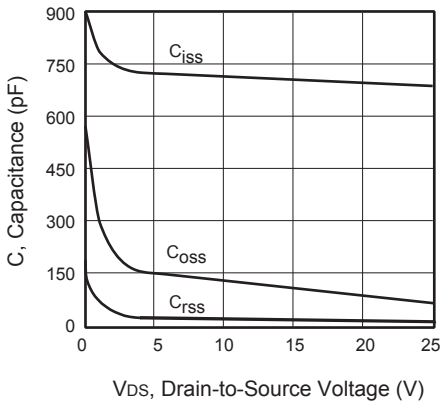
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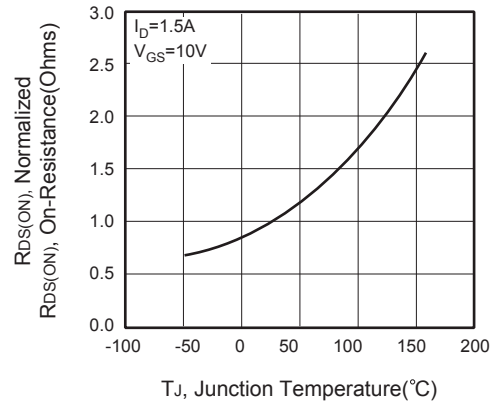
**Figure 1. Output Characteristics**



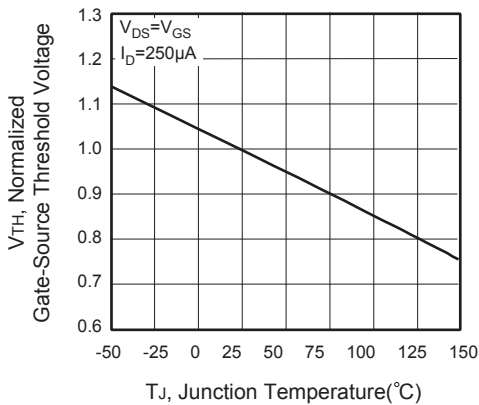
**Figure 2. Transfer Characteristics**



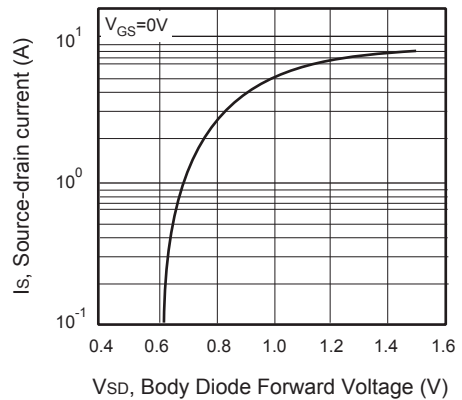
**Figure 3. Capacitance**



**Figure 4. On-Resistance Variation with Temperature**



**Figure 5. Gate Threshold Variation with Temperature**



**Figure 6. Body Diode Forward Voltage Variation with Source Current**



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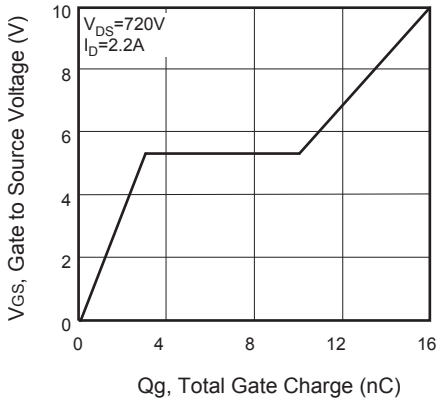


Figure 7. Gate Charge

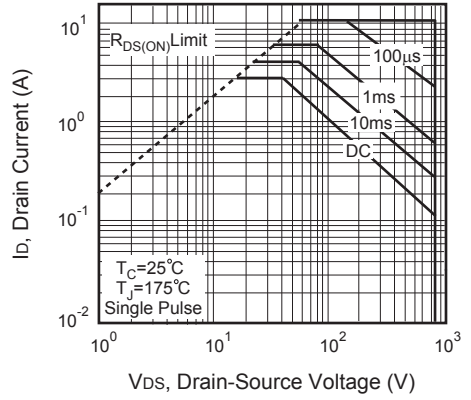


Figure 8. Maximum Safe Operating Area

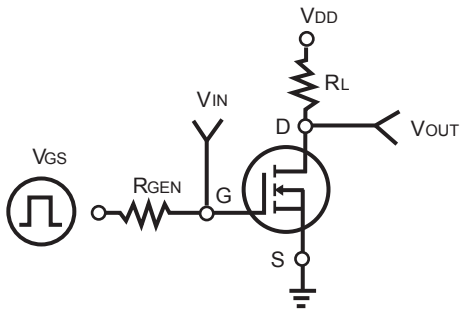


Figure 9. Switching Test Circuit



Figure 10. Switching Waveforms

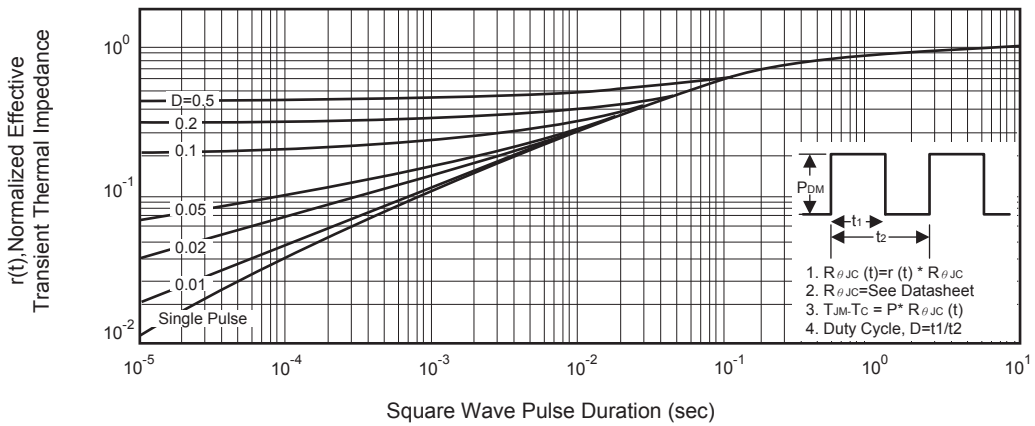


Figure 11. Normalized Thermal Transient Impedance Curve