

MOS Field Effect Transistor

KPA1793

■ Features

● Low on-state resistance

N-channel $R_{DS(on)1} = 69 \text{ m}\Omega$ MAX. ($V_{GS} = 10 \text{ V}$, $I_D = 1.5 \text{ A}$)

$R_{DS(on)2} = 72 \text{ m}\Omega$ MAX. ($V_{GS} = 4.0 \text{ V}$, $I_D = 1.5 \text{ A}$)

$R_{DS(on)3} = 107 \text{ m}\Omega$ MAX. ($V_{GS} = 2.5 \text{ V}$, $I_D = 1.0 \text{ A}$)

● P-channel $R_{DS(on)1} = 115 \text{ m}\Omega$ MAX. ($V_{GS} = -4.5 \text{ V}$, $I_D = -1.5 \text{ A}$)

$R_{DS(on)2} = 120 \text{ m}\Omega$ MAX. ($V_{GS} = -4.0 \text{ V}$, $I_D = -1.5 \text{ A}$)

$R_{DS(on)3} = 190 \text{ m}\Omega$ MAX. ($V_{GS} = -2.5 \text{ V}$, $I_D = -1.0 \text{ A}$)

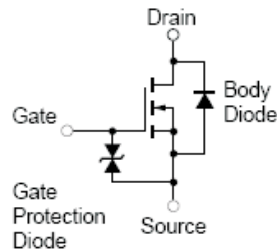
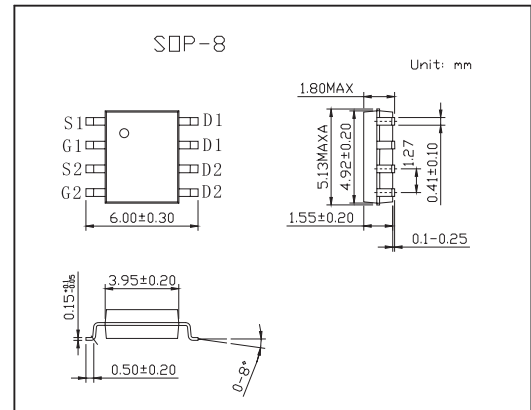
● Low input capacitance

N-channel $C_{iss} = 160 \text{ pF}$ TYP.

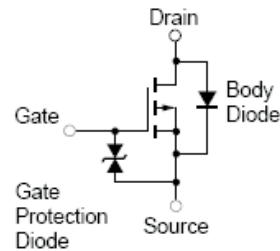
P-channel $C_{iss} = 370 \text{ pF}$ TYP.

● Built-in gate protection diode

● Small and surface mount package



N-Channel



P-Channel

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DS}	20	-20	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GS}	± 12	± 12	V
Drain Current (DC)	$I_{D(DC)}$	± 3	± 3	A
Drain Current (pulse) *1	$I_{D(pulse)}$	± 12	± 12	A
Total Power Dissipation (1 unit) *2	P_T	1.7		W
Total Power Dissipation (2 units) *2	P_T	2		W
Channel Temperature	T_{ch}	150		$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150		$^\circ\text{C}$

*1 $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

*2 Mounted on ceramic substrate of $5500 \text{ mm}^2 \times 2.2 \text{ mm}$

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■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			10	μ A
		V _{DS} = -20V, V _{GS} = 0 V			-10	
Gate Leakage Current	I _{GSS}	V _{GS} = ±12 V, V _{DS} = 0 V			±10	μ A
		V _{GS} = ±12 V, V _{DS} = 0 V			±10	
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	0.5	1.0	1.5	V
		V _{DS} = -10 V, I _D = -1 mA	-0.5	-1.0	-1.5	
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 1.5 A	1.0			S
		V _{DS} = -10 V, I _D = -1.5 A	1.0			
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 4.5 V, I _D = 1.5 A		55	69	mΩ
	R _{DS(on)2}	V _{GS} = 4.0 V, I _D = 1.5 A		57	72	mΩ
	R _{DS(on)3}	V _{GS} = 2.5 V, I _D = 1.0A		78	107	mΩ
	R _{DS(on)1}	V _{GS} = -4.5 V, I _D = -1.5 A		75	115	mΩ
	R _{DS(on)2}	V _{GS} = -4.0 V, I _D = -1.5 A		80	120	mΩ
	R _{DS(on)3}	V _{GS} = -2.5 V, I _D = -1.0 A		116	190	mΩ
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	160		pF
			P- Ch	370		
Output Capacitance	C _{oss}	P- Channel V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	60		pF
			P- Ch	110		
Reverse Transfer Capacitance	C _{rss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	40		pF
			P- Ch	40		
Turn-on Delay Time	t _{d(on)}	N-Channel V _{DD} = 15 V, I _D = 1.5 A, V _{GS} = 4 V	N-Ch	17		ns
			P- Ch	120		
Rise Time	t _r	R _G = 10 Ω	N-Ch	50		ns
			P- Ch	260		
Turn-off Delay Time	t _{d(off)}	P- Channel V _{DD} = -15 V, I _D = -1.5 A, V _{GS} = -4 V	N-Ch	86		ns
			P- Ch	410		
Fall Time	t _f	R _G = 10 Ω	N-Ch	80		ns
			P- Ch	360		
Total Gate Charge	Q _G	N-Channel I _D = 3.0 A, V _{DD} = 16 V, V _{GS} = 4.0 V	N-Ch	3.1		nC
			P- Ch	3.4		
Gate to Source Charge	Q _{GS}	P- Channel I _D = -3.0 A, V _{DD} = -10 V, V _{GS} = -4.0 V	N-Ch	0.7		nC
			P- Ch	1.3		
Gate to Drain Charge	Q _{GD}	I _D = -3.0 A, V _{DD} = -10 V, V _{GS} = -4.0 V	N-Ch	1.4		nC
			P- Ch	1.6		
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 3 A, V _{GS} = 0 V	N-Ch	0.86		V
		I _F = 3 A, V _{GS} = 0 V	P- Ch	0.86		
Reverse Recovery Time	t _{rr}	I _F = 3 A, V _{GS} = 0 V, di/dt = 50 A/μ s	N-Ch	70		ns
			P- Ch	24		
Reverse Recovery Charge	Q _{rr}			12		nC
				1.5		