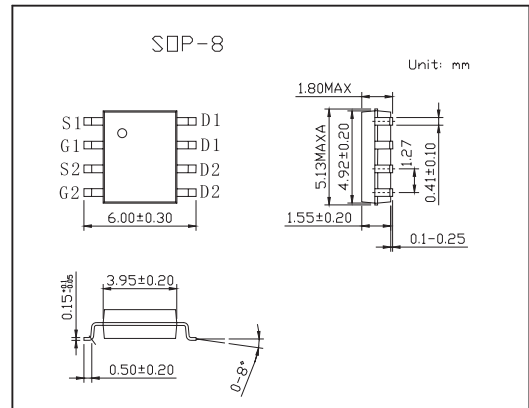
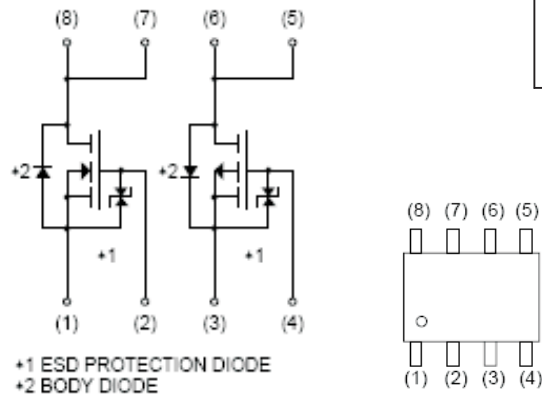


## Switching KP8M7

### ■ Features

- Low on-resistance.
- Built-in G-S Protection Diode.
- Small and Surface Mount Package.
- Power switching, DC / DC converter.



### ■ Absolute Maximum Ratings Ta = 25°C

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-source voltage	V <sub>DSS</sub>	30	-30	V
Gate-source voltage	V <sub>GSS</sub>	±20	±20	V
Drain current Continuous	I <sub>D</sub>	±5.0	±7.0	A
Drain current Pulsed *	I <sub>DP</sub>	±20	±28	A
Source current (Body diode) Continuous	I <sub>S</sub>	1.6	-1.6	A
Source current (Body diode) Pulsed *	I <sub>SP</sub>	6.4	-28	A
Total power dissipation	P <sub>D</sub>	2		W
Channel temperature	T <sub>ch</sub>	150		°C
Storage temperature	T <sub>stg</sub>	-55 to +150		°C
Channel to ambient	R <sub>th (ch-a)</sub>	62.5		°C/W

\* P<sub>w</sub> ≤ 10 μs, Duty cycle ≤ 1%

## KP8M7

## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit	
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	N-Ch		±10	μ A	
		V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	P-Ch		±10		
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	I <sub>D</sub> =1mA, V <sub>GS</sub> =0V	N-Ch	30		V	
		I <sub>D</sub> =-1mA, V <sub>GS</sub> =0V	P-Ch	-30			
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V	N-Ch		1	μ A	
		V <sub>DS</sub> =-30V, V <sub>GS</sub> =0V	P-Ch		-1		
Gate threshold voltage	V <sub>GS (th)</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =1mA	N-Ch	1.0	2.5	V	
		V <sub>DS</sub> =-10V, I <sub>D</sub> =-1mA	P-Ch	-1.0	-2.5		
Static drain-source on-state resistance	R <sub>DS (on)</sub>	I <sub>D</sub> =5.0A, V <sub>GS</sub> =10A	N-Ch		36	51	m Ω
		I <sub>D</sub> =5.0A, V <sub>GS</sub> =4.5V			52	73	
		I <sub>D</sub> =5.0A, V <sub>GS</sub> =4V			58	82	
Static drain-source on-state resistance	R <sub>DS (on)</sub>	I <sub>D</sub> =-7A, V <sub>GS</sub> =-10A	P-Ch		20	28	m Ω
		I <sub>D</sub> =-7A, V <sub>GS</sub> =-4.5V			25	35	
		I <sub>D</sub> =-7A, V <sub>GS</sub> =-4.0V			30	42	
Forward transfer admittance	Y <sub>fs</sub>	I <sub>D</sub> =5.0A, V <sub>DS</sub> =10V	N-Ch	3.0		S	
		I <sub>D</sub> =-7A, V <sub>DS</sub> =-10V	P-Ch	6.0			
Input capacitance	C <sub>iss</sub>	N-Channel V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHz	N-Ch		230	pF	
			P-Ch		2600		
Output capacitance	C <sub>oss</sub>	P-Channel	N-Ch		80	pF	
			P-Ch		450		
Reverse transfer capacitance	C <sub>rss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V, f=1MHz	N-Ch		50	pF	
			P-Ch		350		
Turn-on delay time	t <sub>d (on)</sub>	I <sub>D</sub> =2.5A, V <sub>DD</sub> =15V	N-Ch		6	ns	
		I <sub>D</sub> =-3.5A, V <sub>DD</sub> =-15V	P-Ch		20		
Rise time	t <sub>r</sub>	N-Channel V <sub>GS</sub> =10V, R <sub>L</sub> =6.0 Ω, R <sub>G</sub> =10 Ω	N-Ch		8	ns	
			P-Ch		50		
Turn-off delay time	t <sub>d (off)</sub>	P-Channel	N-Ch		22	ns	
			P-Ch		110		
Fall time	t <sub>f</sub>	V <sub>GS</sub> =-10V, R <sub>L</sub> =4.3 Ω, R <sub>G</sub> =10 Ω	N-Ch		5	ns	
			P-Ch		70		
Total gate charge	Q <sub>g</sub>	N-Channel V <sub>DD</sub> =15V, V <sub>GS</sub> =5V, I <sub>D</sub> =5.0A	N-Ch		3.9	5.5	nC
			P-Ch		25		
Gate-source charge	Q <sub>gs</sub>	P-Channel	N-Ch		1.1		nC
			P-Ch		5.5		
Gate-drain charge	Q <sub>gd</sub>	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-5V, I <sub>D</sub> =-7.0A	N-Ch		1.4		nC
			P-Ch		10		
Forward voltage	V <sub>SD</sub>	I <sub>S</sub> =6.4A, V <sub>GS</sub> =0V	N-Ch		1.2	V	
		I <sub>S</sub> =-1.6A, V <sub>GS</sub> =0V	P-Ch		-1.2		