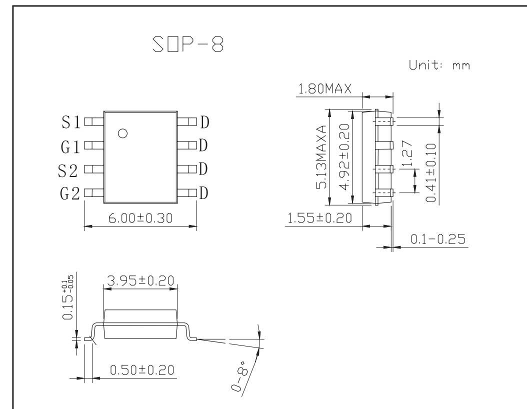
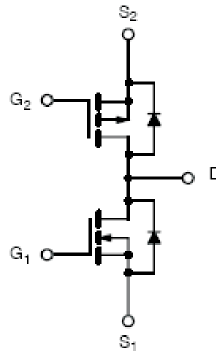
Complementary MOSFET Half-Bridge (N- and P-Channel)

KI4500BDY



■ Features

● TrenchFET Power MOSFET



■ Absolute Maximum Ratings TA = 25℃

Parameter		Symbol	N-Channel		P-Channel		Unit
			10 sec	Steady State	10 sec	Steady State	
Drain-Source Voltage		V_{DS}	20		-20		V
Gate-Source Voltage		V_{GS}	±12		±12		V
Continuous Drain Current (T_J = 150℃)*	T_A = 25℃	I_D	9.1	6.6	?5.3	-3.8	A
	T_A = 70℃		7.3	5.3	-4.9	-3.1	A
Pulsed Drain Current		I_{DM}	30		-20		A
Continuous Source Current (Diode Conduction)*		I_S	2.1	1.1	-2.1	-1.1	A
Maximum Power Dissipation*	T_A = 25℃	P_D	2.5	1.3	2.5	1.3	W
	T_A = 70℃		1.6	0.8	1.6	0.8	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150				℃

*Surface Mounted on FR4 Board;t≤10 sec

■ Thermal Resistance Ratings TA = 25℃

Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ	Max	Typ	Max	
Maximum Junction-to-Ambient*	t ≤10 sec	R_{thJA}	40	50	41	50	℃/W
	Steady State		75	95	75	95	
Maximum Junction-to-Foot	Steady State	R_{thJc}	20	22	23	26	

*Surface Mounted on FR4 Board.

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons		Min	Typ	Max	Unit
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μ A	N-Ch	0.6		1.5	V
		V_{DS} = V_{GS}, I_D = -250 μ A	P-Ch	-0.6		-1.5	
Gate Body Leakage	I_{GSS}	V_{DS} = 0 V V_{GS} = ±12 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0 V	N-Ch			1	
		V_{DS} = -16V, V_{GS} = 0 V	P-Ch			-1	
		V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55℃	N-Ch			5	μ A
		V_{DS} = -16V, V_{GS} = 0 V, T_J = 55℃	P-Ch			-5	
On State Drain Currenta	$I_{D(on)}$	V_{DS} =5 V, V_{GS} = 4.5 V	N-Ch	30			A
		V_{DS} =-5 V, V_{GS} = -4.5 V	P-Ch	-20			
Drain Source On State Resistance*	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 9.1A	N-Ch		0.016	0.020	Ω
		V_{GS} = -4.5 V, I_D = -5.3A	P-Ch		0.048	0.060	
		V_{GS} = 2.5 V, I_D = 3.3A	N-Ch		0.024	0.030	
		V_{GS} = -2.5 V, I_D = -1A	P-Ch		0.082	0.100	
Forward Transconductance*	g_{fs}	V_{DS} = 15 V, I_D = 9.1A	N-Ch		29		mS
		V_{DS} = -15 V, I_D = -5.3A	P-Ch		11		
Diode Forward Voltage*	V_{SD}	I_S = 2.1A, V_{GS} = 0 V	N-Ch		0.8	1.2	V
		I_S = -2.1A, V_{GS} = 0 V	P-Ch		?0.8	-1.2	
Total Gate Charge	Q_g	N-Channel V_{DS} = 10 V, V_{GS} = 4.5V, I_D = 9.1A P-Channel V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -5.3A	N-Ch		11	17	nC
			P-Ch		6.0	9	
Gate Source Charge	Q_{gs}		N-Ch		2.5		
			P-Ch		1.3		
Gate Drain Charge	Q_{gd}		N-Ch		3.2		
			P-Ch		1.6		
Turn On Time	$t_{d(on)}$	N Channel V_{DD} = 10 V, R_L = 10 Ω I_D= 1A, V_{GEN} = 10V, R_g = 6 Ω P-Channel V_{DD} = -10 V, R_L = 10 Ω I_D= -1 A, V_{GEN} = -4.5 V, R_g = 6 Ω	N-Ch		35	50	ns
			P-Ch		20	30	
Rise Time	t_r		N-Ch		50	80	
			P-Ch		35	60	
Turn Off Delay Time	$t_{d(off)}$		N-Ch		31	50	
			P-Ch		55	85	
Fall Time	t_f		N-Ch		15	30	
			P-Ch		35	60	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 2.1A, d_i/d_t = 100 A/ μ s	N-Ch		30	60	
		I_F =- 2.1 A, d_i/d_t = 100 A/ μ s	P-Ch		25	50	

* Pulse test; pulse width ≤300 μ s, duty cycle≤2%.