

Dual N & P-Channel PowerTrench MOSFET

KDS8958

■ Features

● N-Channel

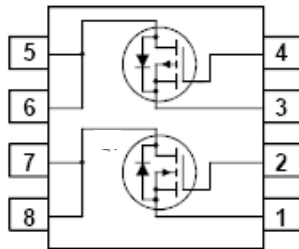
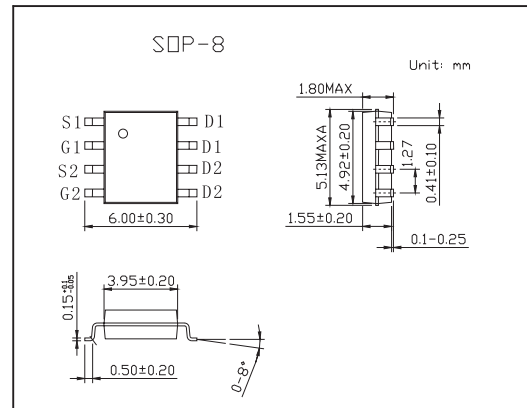
7.0 A, 30 V $R_{DS(ON)} = 0.028 \Omega$ @ $V_{GS} = 10$ V $R_{DS(ON)} = 0.040 \Omega$ @ $V_{GS} = 4.5$ V

● P-Channel

-5 A, -30 V $R_{DS(ON)} = 0.052 \Omega$ @ $V_{GS} = -10$ V $R_{DS(ON)} = 0.080 \Omega$ @ $V_{GS} = -4.5$ V

● Fast switching speed

● High power and handling capability in a widely used surface mount package

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DSS}	30	30	V
Gate to Source Voltage	V_{GS}	± 20	± 20	V
Drain Current Continuous (Note 1a)	I_D	7	-5	A
Drain Current Pulsed		20	-20	A
Power Dissipation for Single Operation	P_D	2		W
Power Dissipation for Single Operation (Note 1a)	P_D	1.6		W
(Note 1b)		1		
(Note 1c)		0.9		
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150		$^\circ\text{C}$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78		$^\circ\text{C/W}$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40		$^\circ\text{C/W}$

KDS8958

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250 μ A	N-Ch	30		V	
		V _{GS} = 0 V, I _D = -250 μ A	P-Ch	-30			
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D = 250 μ A, Referenced to 25°C	N-Ch		25	mV/°C	
		I _D = -250 μ A, Referenced to 25°C	P-Ch		-22		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V, V _{GS} = 0 V	N-Ch		1	μ A	
		V _{DS} = -24 V, V _{GS} = 0 V	P-Ch		-1		
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0 V	N-Ch		±100	nA	
		V _{GS} = ±20 V, V _{DS} = 0 V	P-Ch		±100		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μ A	N-Ch	1	1.6	3	V
		V _{DS} = V _{GS} , I _D = -250 μ A	P-Ch	-1	-1.7	-3	
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I _D = 250 μ A, Referenced to 25°C	N-Ch		-4.3	mV/°C	
		I _D = -250 μ A, Referenced to 25°C	P-Ch		4		
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7A	N-Ch		21	28	m Ω
		V _{GS} = 10 V, I _D = 7 A, T _J = 125°C			32	42	
		V _{GS} = 4.5 V, I _D = 6 A			27	40	
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -5 A	P-Ch		41	52	
		V _{GS} = -10 V, I _D = -5 A, T _J = 125°C			58	78	
		V _{GS} = -4.5 V, I _D = -4A			58	80	
On-State Drain Current	I _{D(on)}	V _{GS} = 10 V, V _{DS} = 5V	N-Ch	20		A	
		V _{GS} = -10 V, V _{DS} = -5V	P-Ch	-20			
Forward Transconductance	g _{FS}	V _{DS} = 5V, I _D = 7A	N-Ch		19	S	
		V _{DS} = -5V, I _D = -5A	P-Ch		11		
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		789	pF	
			P-Ch		690		
Output Capacitance	C _{oss}	P-Channel	N-Ch		173	pF	
			P-Ch		306		
Reverse Transfer Capacitance	C _{rss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		66	pF	
			P-Ch		77		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, I _D = 1 A,	N-Ch		6	12	ns
			P-Ch		6.7	13.4	
Turn-On Rise Time	t _r	V _{GS} = 10 V, R _{GEN} = 6 Ω (Note 2)	N-Ch		10	18	ns
			P-Ch		9.7	19.4	
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = -10 V, I _D = -1 A,	N-Ch		18	29	ns
			P-Ch		19.8	35.6	
Turn-Off Fall Time	t _f	V _{GS} = -10 V, R _{GEN} = 6 Ω (Note 2)	N-Ch		5	12	ns
			P-Ch		12.3	22.2	
Total Gate Charge	Q _g	N-Channel V _{DS} = 15V, I _D = 7A, V _{GS} = 10V (Note 2)	N-Ch		16	26	nC
			P-Ch		14	23	
Gate-Source Charge	Q _{gs}	P-Channel	N-Ch		2.5	nC	
			P-Ch		2.2		
Gate-Drain Charge	Q _{gd}	V _{DS} = -15V, I _D = -5A, V _{GS} = -10V (Note 2)	N-Ch		2.1	nC	
			P-Ch		1.9		

KDS8958

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Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Maximum Continuous Drain-Source Diode Forward Current	Is	N-Ch			1.3	A
		P-Ch			-1.3	
Drain-Source Diode Forward Voltage	VSD	VGS = 0 V, Is = 1.3A (Not 2)		0.74	1.2	V
		VGS = 0 V, Is = -1.3A (Not 2)		-0.76	-1.2	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°/W when mounted on a .02 in² pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%