

60V Complementary PowerTrench MOSFET

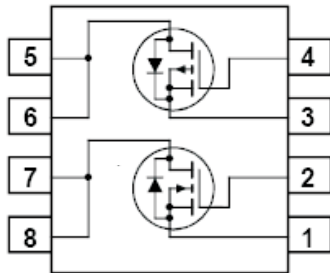
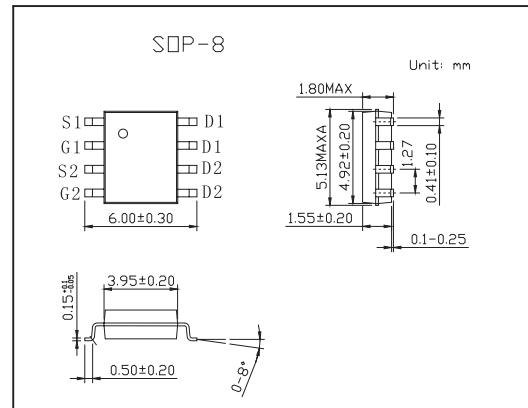
KDS4559

■ Features

● N-Channel

4.5 A, 60 V $R_{DS(ON)} = 55\text{m}\Omega$ @ $V_{GS} = 10\text{V}$ $R_{DS(ON)} = 75\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$

● P-Channel

-3.5 A, -60 V $R_{DS(ON)} = 105\text{m}\Omega$ @ $V_{GS} = -10\text{V}$ $R_{DS(ON)} = 135\text{m}\Omega$ @ $V_{GS} = -4.5\text{V}$ ■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	N-Channel	P- Channel	Unit
Drain to Source Voltage	V_{DS}	60	-60	V
Gate to Source Voltage	V_{GS}	± 20	± 20	V
Drain Current Continuous (Note 1a)	I_D	4.5	-3.5	A
Drain Current Pulsed		20	-20	A
Power Dissipation for Single Operation	P_D	2		W
Power Dissipation for Single Operation (Note 1a)	P_D	1.6		W
(Note 1b)		1.2		
(Note 1c)		1		
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175		$^\circ\text{C}$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78		$^\circ\text{C}/\text{W}$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40		$^\circ\text{C}/\text{W}$

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■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit	
Single Pulse Drain-Source Avalanche Energy	WDSS	V _{DD} = 30 V, I _D = 4.5 A			90	mJ	
Maximum Drain-Source Avalanche Current	I _{AR}				4.5	A	
Drain-Source Breakdown Voltage	B _V DSS	V _{GS} = 0 V, I _D = 250 μA	N-Ch	60		V	
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-60			
Breakdown Voltage Temperature Coefficient	$\frac{\Delta B_{V_{DSS}}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C	N-Ch		58	mV/°C	
		I _D = -250 μA, Referenced to 25°C	P-Ch		-49		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48V, V _{GS} = 0 V	N-Ch		1	μA	
		V _{DS} = -48 V, V _{GS} = 0 V	P-Ch		-1		
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V, V _{DS} = 0 V	N-Ch		±100	nA	
		V _{GS} = ±20 V, V _{DS} = 0 V	P-Ch		±100		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1	2.2	3	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1	-1.6	-3	
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C	N-Ch		-5.5	mV/°C	
		I _D = -250 μA, Referenced to 25°C	P-Ch		4		
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.5A	N-Ch		42	55	mΩ
		V _{GS} = 10 V, I _D = 4.5 A, T _J = 125°C			72	94	
		V _{GS} = 4.5 V, I _D = 4 A			55	75	
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -3.5 A	P-Ch		82	105	
		V _{GS} = -10 V, I _D = -3.5 A, T _J = 125°C			130	190	
		V _{GS} = -4.5 V, I _D = -3.1A			105	135	
On-State Drain Current	I _{D(on)}	V _{GS} = 10 V, V _{DS} = 5V	N-Ch	20		A	
		V _{GS} = -10 V, V _{DS} = -5V	P-Ch	-20			
Forward Transconductance	g _{FS}	V _{DS} = 10V, I _D = 4.5A	N-Ch		14	S	
		V _{DS} = -5V, I _D = -3.5A	P-Ch		9		
Input Capacitance	C _{iss}	N-Channel V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		650	pF	
			P-Ch		759		
Output Capacitance	C _{oss}	P-Channel	N-Ch		80	pF	
			P-Ch		90		
Reverse Transfer Capacitance	C _{rss}	V _{DS} = -30 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		35	pF	
			P-Ch		39		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 30 V, I _D = 1 A,	N-Ch		11	20	ns
			P-Ch		7	14	
Turn-On Rise Time	t _r	V _{GS} = 10 V, R _{GEN} = 6 Ω (Note 2)	N-Ch		8	18	ns
			P-Ch		10	20	
Turn-Off Delay Time	t _{d(off)}	P-Channel V _{DD} = -30 V, I _D = -1 A,	N-Ch		19	35	ns
			P-Ch		19	34	
Turn-Off Fall Time	t _f	V _{GS} = -10 V, R _{GEN} = 6 Ω (Note 2)	N-Ch		6	15	ns
			P-Ch		12	22	
Total Gate Charge	Q _g	N-Channel V _{DS} = 30V, I _D = 4.5A, V _{GS} = 10V	N-Ch		12.5	18	nC
			P-Ch		15	21	
Gate-Source Charge	Q _{gs}	(Note 2) P-Channel	N-Ch		2.4	nC	
			P-Ch		2.5		
Gate-Drain Charge	Q _{gd}	V _{DS} = -30V, I _D = -3.5A, V _{GS} = -10V (Note 2)	N-Ch		2.6	nC	
			P-Ch		3.0		

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Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Maximum Continuous Drain-Source Diode Forward Current	Is	N-Ch			1.3	A
		P-Ch			-1.3	
Drain-Source Diode Forward Voltage	VSD	VGS = 0 V, Is = 1.3A (Not 2)		0.8	1.2	V
		VGS = 0 V, Is = -1.3A (Not 2)		-0.8	-1.2	

Notes:

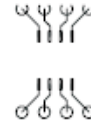
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°C/W when mounted on a .02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%