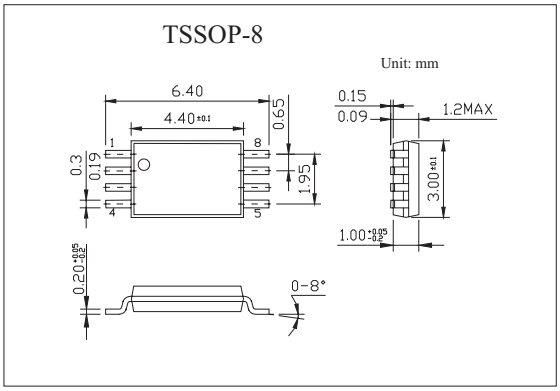
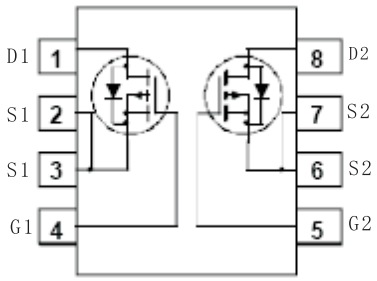
Dual P-Channel 2.5V Specified PowerTrench MOSFET

KDW2504P



■ Features

- -3.8 A, - 20 V. $R_{DS(ON)}$ = 0.043Ω @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 0.070Ω @ V_{GS} =-2.5V
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- Extended VGSS range (±12V) for battery applications



■ Absolute Maximum Ratings Ta = 25℃

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	-20	V
Gate to Source Voltage	V_{GS}	±12	V
Drain Current Continuous (Note 1a)	I_D	-3.8	A
Drain Current Pulsed		-30	A
Power Dissipation for Single Operation (Note 1a)	P_D	1	W
Power Dissipation for Single Operation (Note 1b)		0.6	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	℃
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	125	℃/W
Thermal Resistance Junction to Ambient (Note 1b)	$R_{\theta JA}$	208	℃/W

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■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	B_{VDSS}	V_{GS} = 0 V, I_D = -250 μA	-20			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D = -250 μA, Referenced to 25℃		-16		mV/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
Gate-Body Leakage, Forward	I_{GSSF}	V_{GS} = -12 V, V_{DS} = 0 V			-100	nA
Gate-Body Leakage, Reverse	I_{GSSR}	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 μA	-0.6	-1	-1.5	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D = -250 μA, Referenced to 25℃		3		mV/℃
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} =-4.5 V, I_D =-3.8 A		0.036	0.043	Ω
		V_{GS} = -2.5 V, I_D = -3.0 A		0.056	0.070	
		V_{GS} = -4.5 V, I_D =-3.8 A,TJ = 125℃		0.049	0.069	
On-State Drain Current	$I_{D(on)}$	V_{GS} = -4.5 V, V_{DS} = -5V	-15			A
Forward Transconductance	g_{FS}	V_{DS} = -5 V, I_D = -3.5A		13.2		S
Input Capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V,f = 1.0 MHz		1015		pF
Output Capacitance	C_{oss}			446		pF
Reverse Transfer Capacitance	C_{rss}			118		pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -5 V, I_D = -1 A,V_{GS} = -4.5 V, R_{GEN} = 6 Ω		11	20	ns
Turn-On Rise Time	tr			18	32	ns
Turn-Off Delay Time	$t_{d(off)}$			34	55	ns
Turn-Off Fall Time	tf			34	55	ns
Total Gate Charge V_{gs}=5V	Q_g	V_{DS} = -5 V, I_D = -3.8 A,V_{GS}=-4.5V(Note 2)		9.7	16	nC
Gate-Source Charge	Q_{gs}			2.2		nC
Gate-Drain Charge	Q_{gd}			2.4		nC
Maximum Continuous Drain-Source Diode Forward Current	I_S				-0.83	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S =- 0.83 A (Note 2)		-0.7	-1.2	V

Notes:

1 $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ is 125℃/W (steady state) when mounted on a 1 $inch^2$ copper pad on FR-4.

b) $R_{\theta JA}$ is 208 ℃/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width ＜ 300 μs, Duty Cycle ＜ 2.0%