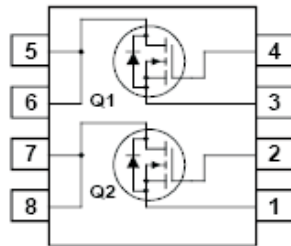
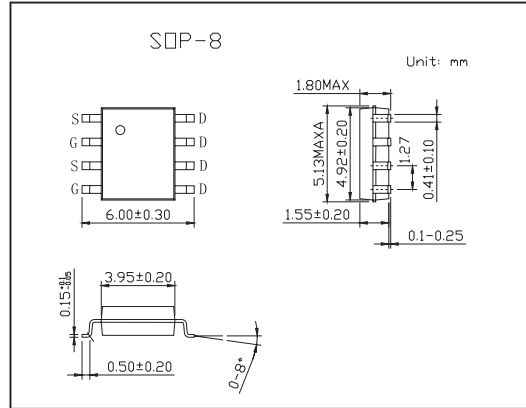


Dual N-Channel Logic Level PowerTrench MOSFET

KDS6910

■ Features

- 7.5 A, 30 V. $R_{DS(ON)} = 13\text{m}\Omega$ @ $V_{GS} = 10\text{V}$
 $R_{DS(ON)} = 17\text{m}\Omega$ @ $V_{GS} = 4.5\text{V}$
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GS}	± 20	V
Drain Current Continuous (Note 1a)	I_D	7.5	A
Drain Current Pulsed		20	A
Power Dissipation for Single Operation (Note 1a)	P_D	1.6	W
Power Dissipation for Single Operation (Note 1b)		1	
Power Dissipation for Single Operation (Note 1c)		0.9	
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Thermal Resistance Junction to Case (Note 1)	$R_{\theta JC}$	40	$^\circ\text{C/W}$
Thermal Resistance Junction to Ambient (Note 1a)	$R_{\theta JA}$	78	$^\circ\text{C/W}$

KDS6910

■ Electrical Characteristics Ta = 25°C

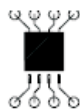
Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250 μA	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C		28		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V			1	μA
		V _{DS} = 24 V, V _{GS} = 0 V, T _J = 55°C			10	
Gate-Body Leakage, Forward	I _{GSSF}	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
Gate-Body Leakage, Reverse	I _{GSSR}	V _{GS} = -20 V, V _{DS} = 0 V			-100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	1.8	3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I _D = 250 μA, Referenced to 25°C		-4.7		mV/°C
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 7.5 A		10.6	13	mΩ
		V _{GS} = 4.5 V, I _D = 6.5 A		13	17	
		V _{GS} = 10 V, I _D = 7.5 A, T _J = 125°C		14.5	20	
On-State Drain Current	I _{D(on)}	V _{GS} = 10 V, V _{DS} = 5V	20			A
Forward Transconductance	g _{FS}	V _{DS} = 5 V, I _D = 7.5A		36		S
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz		1130		pF
Output Capacitance	C _{oss}			300		pF
Reverse Transfer Capacitance	C _{rss}			100		pF
Gate Resistance	R _G	V _{GS} = 15 mV, f = 1.0 MHz		2.4		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		9	18	ns
Turn-On Rise Time	t _r			5	10	ns
Turn-Off Delay Time	t _{d(off)}			26	42	ns
Turn-Off Fall Time	t _f			7	14	ns
Total Gate Charge at V _{GS} =10V	Q _{g(TOT)}				17	24
Total Gate Charge V _{GS} =5V	Q _g	V _{DS} = 15 V, I _D = 7.5 A (Note 2)		9	13	nC
Gate-Source Charge	Q _{gs}			3.1		nC
Gate-Drain Charge	Q _{gd}			2.7		nC
Maximum Continuous Drain-Source Diode Forward Current	I _S				1.3	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 1.3 A (Not 2)			1.2	V
Diode Reverse Recovery Time	t _{rr}	I _F = 7.5A		24		nS
Diode Reverse Recovery Charge	Q _{rr}	di _F /dt = 100 A/μs		13		nC

Notes:

1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%