

## MOS Field Effect Transistor

## KPA1716

## ■ Features

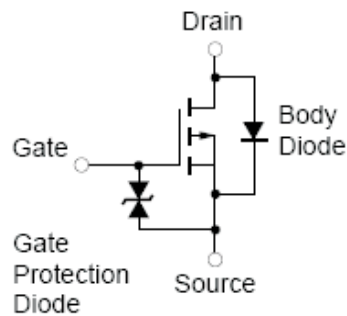
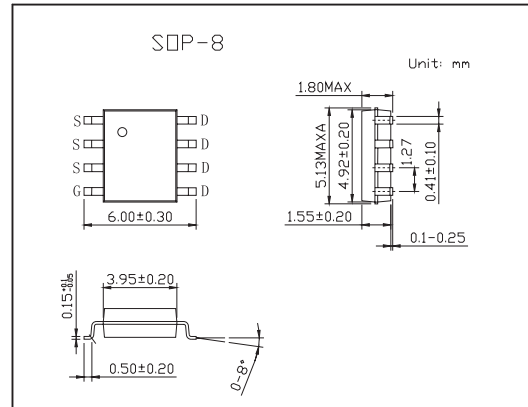
- Low on-state resistance

$R_{DS(on)1} = 12.5 \text{ m}\Omega$  TYP. ( $V_{GS} = -10 \text{ V}$ ,  $I_D = -4 \text{ A}$ )

$R_{DS(on)2} = 17 \text{ m}\Omega$  TYP. ( $V_{GS} = -4.5 \text{ V}$ ,  $I_D = -4 \text{ A}$ )

$R_{DS(on)3} = 19 \text{ m}\Omega$  TYP. ( $V_{GS} = -4.01 \text{ V}$ ,  $I_D = -4 \text{ A}$ )

- Low  $C_{iss}$  :  $C_{iss} = 2100 \text{ pF}$  TYP.
- Built-in G-S protection diode
- Small and surface mount package

■ Absolute Maximum Ratings  $T_a = 25^\circ\text{C}$ 

Parameter	Symbol	Rating	Unit
Drain to Source Voltage ( $V_{GS} = 0$ )	$V_{DSS}$	-30	V
Gate to Source Voltage ( $V_{DS} = 0$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) $T_a = 25^\circ\text{C}$	$I_{D(DC)}$	$\pm 8$	A
Drain Current (Pulse) *1	$I_{D(pulse)}$	$\pm 32$	A
Total Power Dissipation $T_a = 25^\circ\text{C}$ *2	$P_T$	2.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to + 150	$^\circ\text{C}$

\*1  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$

\*2 Mounted on ceramic substrate of  $1200\text{mm}^2 \times 1.0 \text{ mm}$

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## ■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>DS</sub> = -10V, I <sub>D</sub> = -4.0 A		12.5	16	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -4.0 A		17	23	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = -4.0V, I <sub>D</sub> = -4.0 A		19	26	mΩ
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = 1 mA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = -4.0A	7	14		S
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0			-1	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0, f = 1 MHz		2100		pF
Output Capacitance	C <sub>oss</sub>			700		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			300		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = -4.0 A, V <sub>GS(on)</sub> = -10 V, V <sub>DD</sub> = -15 V, R <sub>G</sub> = 10 Ω		30		ns
Rise Time	t <sub>r</sub>			150		ns
Turn-off Delay Time	t <sub>d(off)</sub>			120		ns
Fall Time	t <sub>f</sub>			76		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = -8.0A, V <sub>DD</sub> = -24V, V <sub>GS</sub> = -10 V		40		nC
Gate to Source Charge	Q <sub>GS</sub>			6		nC
Gate to Drain Charge	Q <sub>GD</sub>			10		nC
Body Diode forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 8.0 A, V <sub>GS</sub> = 0		0.8		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 8.0 A, V <sub>GS</sub> = 0 V		45		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/μs		33		nC