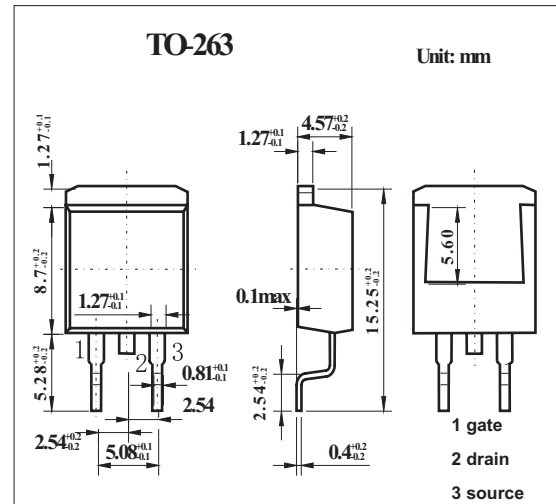
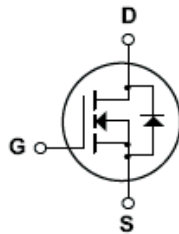


200V N-Channel MOSFET KQB630

■ Features

- 9A, 200 V. $R_{DS(ON)} = 0.4 \Omega$ @ $V_{GS} = 10 V$
- Low gate charge (typical 19nC)
- Low C_{rss} (typical 35pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



■ Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	200	V
Drain Current Continuous ($T_c=25^\circ C$)	I_D	9	A
Drain Current Continuous ($T_c=100^\circ C$)		5.7	A
Drain Current Pulsed *1	I_{DM}	36	A
Gate-Source Voltage	V_{GSS}	± 25	V
Single Pulsed Avalanche Energy*2	E_{AS}	162	mJ
Avalanche Current *1	I_{AR}	9	A
Repetitive Avalanche Energy *1	E_{AR}	7.8	mJ
Peak Diode Recovery dv/dt *3	dv/dt	5.5	V/ns
Power dissipation @ $T_A=25^\circ C$	P_D	3.13	W
Power dissipation @ $T_c=25^\circ C$		78	W
Derate above $25^\circ C$		0.62	W/ $^\circ C$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	$^\circ C$
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	T_L	300	$^\circ C$
Thermal Resistance Junction to Case	$R_{\theta JC}$	1.61	$^\circ C/W$
Thermal Resistance Junction to Ambient *4	$R_{\theta JA}$	40	$^\circ C/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ C/W$

*1 Repetitive Rating: Pulse width limited by maximum junction temperature

*2 $I = 3mH, I_{AS} = 9A, V_{DD} = 50V, R_G = 25 \Omega, \text{Startion } T_J = 25^\circ C$

*3 $I_{SD} \leq 9A, di/dt \leq 300A/\mu S, V_{DD} \leq V_{DSS}, \text{Startiong } T_J = 25^\circ C$

*4 When mounted on the minimum pad size recommended (PCB Mount)

KQB630

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BVDSS	V _{GS} = 0 V, I _D = 250 μ A	200			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BVDSS}{\Delta T_J}$	I _D = 250 μ A, Referenced to 25°C		0.20		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V			1	μ A
		V _{DS} = 160 V, T _C = 125°C			10	μ A
Gate-Body Leakage Current, Forward	I _{GSSF}	V _{GS} = 25 V, V _{DS} = 0 V			100	nA
Gate-Body Leakage Current, Reverse	I _{GSSR}	V _{GS} = -25 V, V _{DS} = 0 V			-100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μ A	2.0		4.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.5A		0.34	2.0	Ω
Forward Transconductance	g _{FS}	V _{DS} = 40 V, I _D = 4.5A *		4.4		S
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		420	550	pF
Output Capacitance	C _{oss}			85	110	pF
Reverse Transfer Capacitance	C _{rss}			35	45	pF
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, I _D = 9A, R _G = 25 Ω *		8	30	ns
Turn-On Rise Time	t _r			75	160	ns
Turn-Off Delay Time	t _{d(off)}			47	110	ns
Turn-Off Fall Time	t _f			64	140	ns
Total Gate Charge	Q _g				19	25
Gate-Source Charge	Q _{gs}	V _{DS} = 160 V, I _D = 9A, V _{GS} = 10 V *		3		nC
Gate-Drain Charge	Q _{gd}			9.5		nC
Maximum Continuous Drain-Source Diode Forward Current	I _S				9	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				36	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 9A *			1.5	V
Diode Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, dI _F /dt = 100 A/μ s, I _S = 9A		150		ns
Diode Reverse Recovery Current	Q _{rr}			0.68		μ C

* Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle ≤ 2.0%