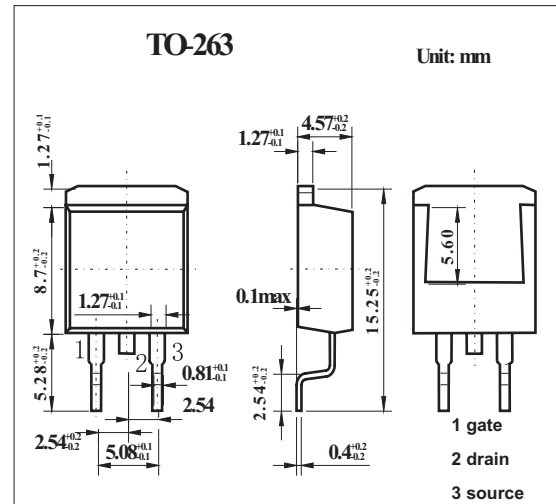
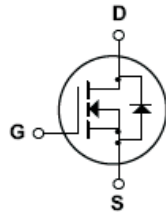


500V N-Channel MOSFET KQB9N50

■ Features

- 9A, 500 V. $R_{DS(ON)} = 0.73 \Omega$ @ $V_{GS} = 10 V$
- Low gate charge (typical 28nC)
- Low Crss(typical 20 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



■ Absolute Maximum Ratings $T_a = 25^\circ C$

Parameter	Symbol	Rating	Unit
Drain to Source Voltage	V_{DSS}	500	V
Drain Current Continuous ($T_c=25^\circ C$)	I_D	9	A
Drain Current Continuous ($T_c=100^\circ C$)		5.7	A
Drain Current Pulsed *1	I_{DM}	36	A
Gate-Source Voltage	V_{GSS}	± 30	V
Single Pulsed Avalanche Energy*2	EAS	360	mJ
Avalanche Current *1	I_{AR}	9	A
Repetitive Avalanche Energy *1	EAR	14.7	mJ
Peak Diode Recovery dv/dt *3	dv/dt	4.5	V/ns
Power dissipation @ $T_A=25^\circ C$	P_D	3.13	W
Power dissipation @ $T_c=25^\circ C$ Derate above $25^\circ C$		1.18	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	°C
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	T_L	300	°C
Thermal Resistance Junction to Case	$R_{\theta JC}$	0.85	°C/W
Thermal Resistance Junction to Ambient *4	$R_{\theta JA}$	40	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	62.5	°C/W

*1 Repetitive Rating: Pulse width limited by maximum junction temperature

*2 $I=8mA, I_{AS}=9A, V_{DD}=50V, R_G=25 \Omega, Startion T_J=25^\circ C$

*3 $I_{SD} \leq 9A, di/dt \leq 200A/\mu S, V_{DD} \leq V_{DSS}, Startiong T_J=25^\circ C$

*4 When mounted on the minimum pad size recommended (PCB Mount)

KQB9N50

■ Electrical Characteristics Ta = 25°C

Parameter	Symbol	Testconditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0 V, I _D = 250 μ A	500			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I _D = 250 μ A, Referenced to 25°C		0.55		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V			1	μ A
		V _{DS} = 400 V, T _C = 125°C			10	μ A
Gate-Body Leakage Current, Forward	I _{GSSF}	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
Gate-Body Leakage Current, Reverse	I _{GSSR}	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μ A	3.0		5.0	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.5A		0.58	0.73	Ω
Forward Transconductance	g _{FS}	V _{DS} = 50 V, I _D = 4.5A *		8.2		S
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		1100	1450	pF
Output Capacitance	C _{oss}			160	210	pF
Reverse Transfer Capacitance	C _{rss}			20	30	pF
Turn-On Delay Time	t _{d(on)}	V _{DD} = 250 V, I _D = 9.0A, R _G = 25 Ω *		25	60	ns
Turn-On Rise Time	t _r			95	200	ns
Turn-Off Delay Time	t _{d(off)}			55	120	ns
Turn-Off Fall Time	t _f			60	130	ns
Total Gate Charge	Q _g	V _{DS} = 400 V, I _D = 9.0A, V _{GS} = 10 V *		28	36	nC
Gate-Source Charge	Q _{gs}			7.0		nC
Gate-Drain Charge	Q _{gd}			12.5		nC
Maximum Continuous Drain-Source Diode Forward Current	I _S				9.0	A
Maximum Pulsed Drain-Source Diode Forward Current	I _{SM}				36	A
Drain-Source Diode Forward Voltage	V _{SD}	V _{GS} = 0 V, I _S = 9.0 A			1.4	V
Diode Reverse Recovery Time	t _{rr}	V _{GS} = 0 V, dI _F /dt = 100 A/μ s, I _S = 9.0A *		300		ns
Diode Reverse Recovery Current	Q _{rr}				2.2	

* Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle ≤ 2.0%