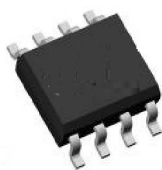
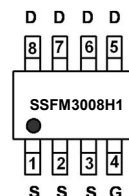


Main Product Characteristics

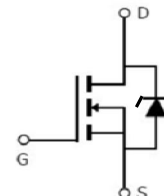
V_{DSS}	30V
$R_{DS(on)}$	7.4mohm(typ.)
I_D	20A



SOP-8



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature
- Lead free product



Description

It utilizes the latest FRRMOS (fast reverse recovery MOS) trench processing techniques to achieve the high cell density and reduces the on-resistance, fast switching and soft reverse recovery time. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute Max Rating

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	20	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	16	
I_{DM}	Pulsed Drain Current②	136	
$P_D @ TC = 25^\circ C$	Power Dissipation③	3.1	W
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy @ $L=0.1mH$	100	mJ
I_{AS}	Avalanche Current @ $L=0.1mH$	44	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ C$

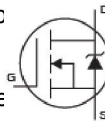
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case③	—	22	$^\circ C/W$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	35	$^\circ C/W$
	Junction-to-Ambient (PCB mounted, steady-state) ④	—	65	$^\circ C/W$

Electrical Characteristics @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

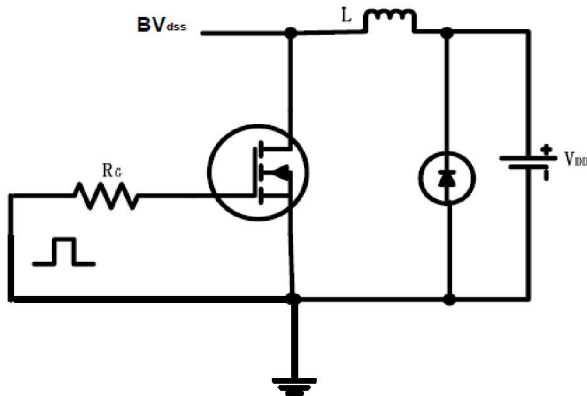
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	30	36.5	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	7.4	8	$m\Omega$	$V_{GS}=10V, I_D=20A$
		—	11.5	14	$m\Omega$	$V_{GS}=4.5V, I_D=10A$
$V_{GS(th)}$	Gate threshold voltage	1	—	3	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source leakage current	—	—	10	μA	$V_{DS} = 30V, V_{GS} = 0V$
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 20V$
		-100	—	—		$V_{GS} = -20V$
G_{fs}	Forward Transconductance	4	7.6	—	S	$V_{DS}= 15V, I_D=16A$
Q_g	Total gate charge	—	17.6	—	nC	$V_{DS}=15V,$ $I_D=16A,$ $V_{GS}=4.5V$
Q_{gs}	Gate-to-Source charge	—	6.5	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	8.6	—		
$t_{d(on)}$	Turn-on delay time	—	32.8	—	ns	$V_{GS}=4.5V, V_{DS}=15V,$ $R_{GEN}=3\Omega, I_D=16A$
t_r	Rise time	—	104.3	—		
$t_{d(off)}$	Turn-Off delay time	—	12.9	—		
t_f	Fall time	—	8.5	—		
C_{iss}	Input capacitance	—	1844	—	pF	$V_{GS} = 0V$ $V_{DS} = 15V$ $f = 1MHz$
C_{oss}	Output capacitance	—	342	—		
C_{rss}	Reverse transfer capacitance	—	215	—		

Source-Drain Ratings and Characteristics

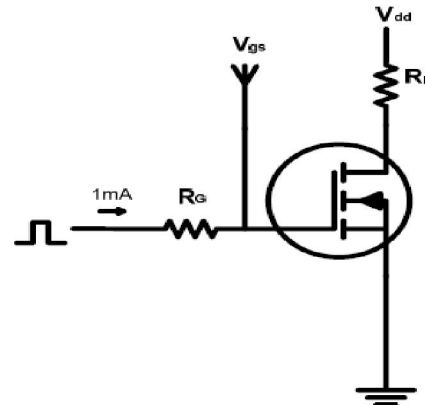
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	—	—	20	A	MOSFET symbt showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current	—	—	136	A	
V_{SD}	Diode Forward Voltage	—	0.7	1.0	V	$I_S=1.0A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	16.5	—	ns	$T_J = 25^{\circ}\text{C}, I_F = 3A, di/dt =$
Q_{rr}	Reverse Recovery Charge	—	8.2	—	nC	$100A/\mu s$

Test Circuits and Waveforms

EAS test circuits:



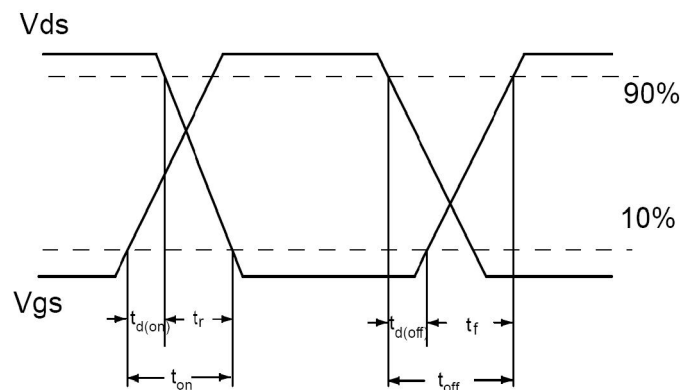
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-ambient thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 175^\circ\text{C}$.

Typical Electrical Characteristics

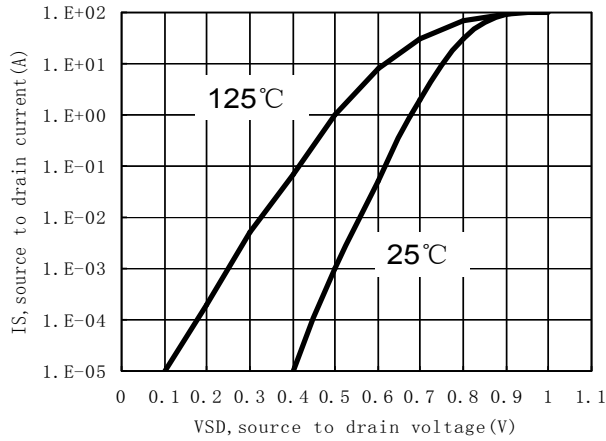


Figure 1: Body-Diode Characteristics

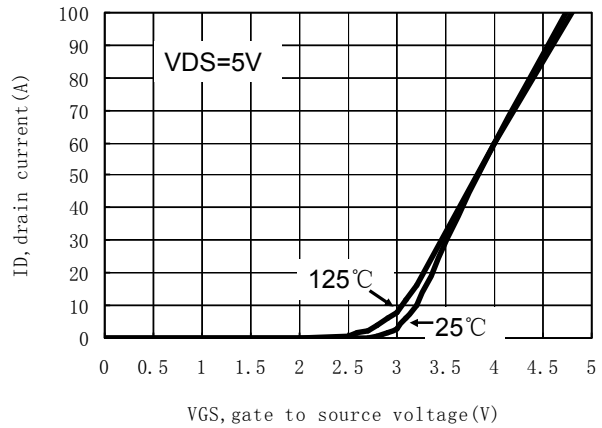


Figure 2: Typical Transfer Characteristics

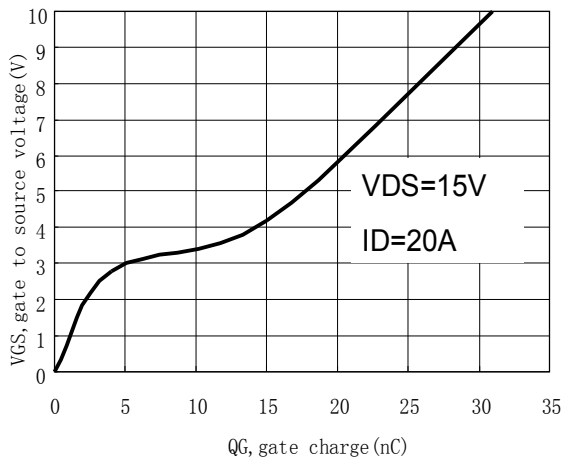


Figure 3: Gate-Charge Characteristics

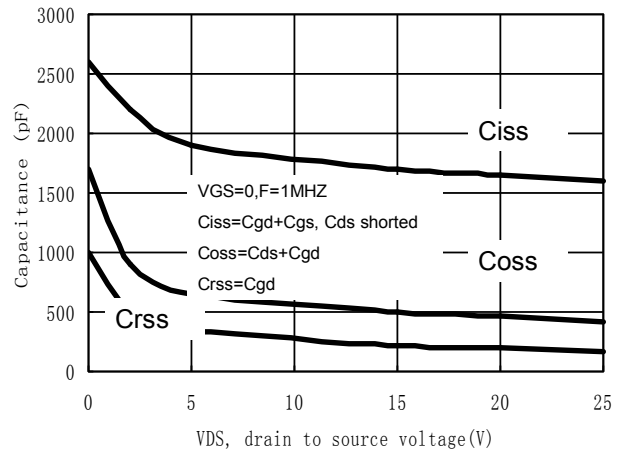


Figure 4: Capacitance Characteristics

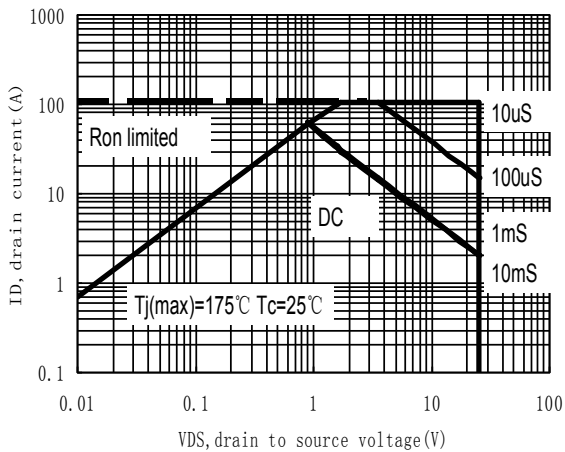


Figure 5: Maximum Forward Biased Safe Operating Area

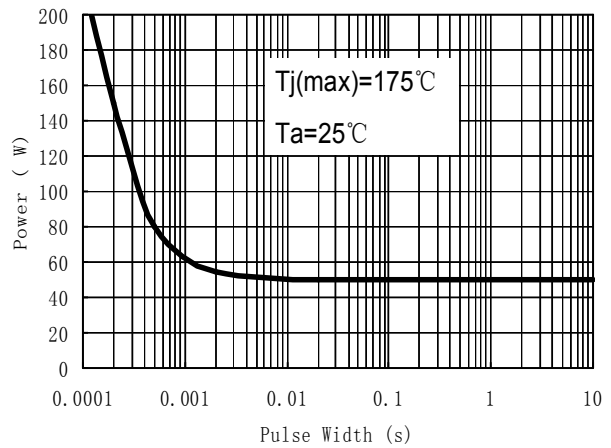


Figure 6: Single Pulse Power Rating Junction-to-Case

Typical Thermal Characteristics

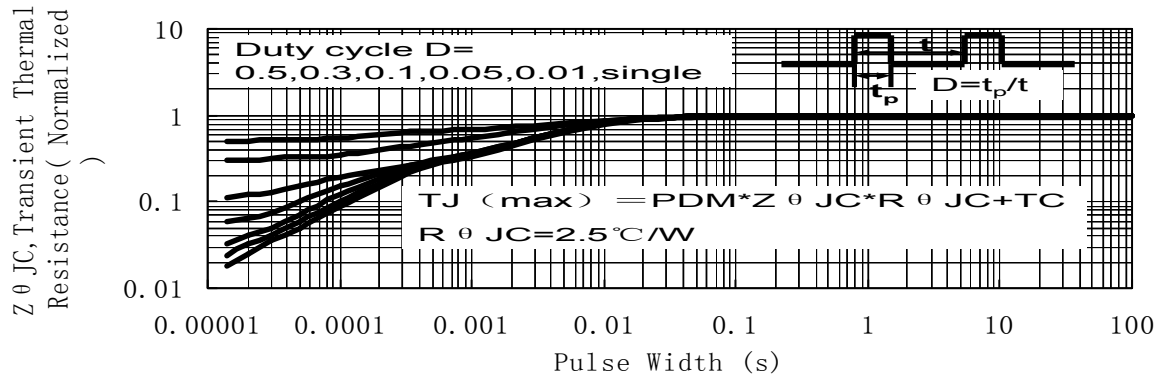
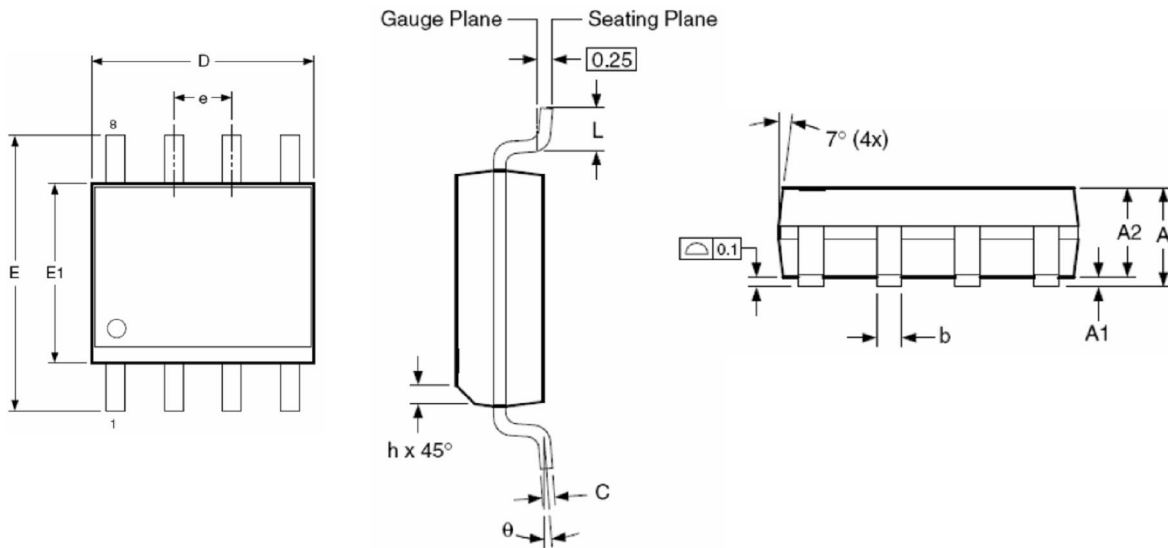


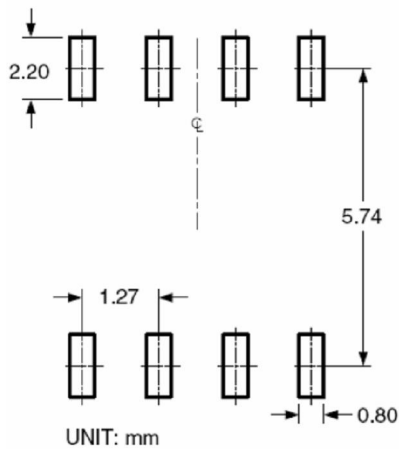
Figure 7: Normalized Thermal transient Impedance Curve

Mechanical Data

SOP-8 PACKAGE INFORMATION



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

Notes:

1. Dimensions are inclusive of plating
2. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
3. Dimension L is measured in gauge plane.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.



Ordering and Marking Information

Device Marking: SSFM3008H1

Package (Available)

SOP-8

Operating Temperature Range

C : -55 to 175 °C

Devices per Unit

Package Type	Units/ Tube	Tubes/ Inner Box	Units/Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
SOP-8	2500	2	5000	8	40000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices