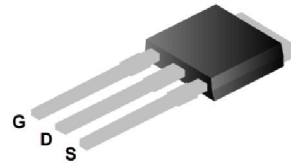
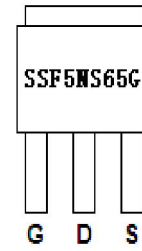


Main Product Characteristics

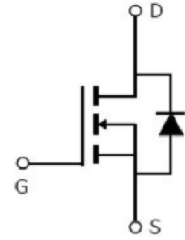
V_{DSS}	650V
$R_{DS(on)}$	1.0Ω (typ.)
I_D	5A ①



TO-251



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Lead free product



Description

The SSF5NS65G series MOSFETs is a new technology, which combines an innovative super junction technology and advance process. This new technology achieves low $R_{DS(ON)}$, energy saving, high reliability and uniformity, superior power density and space saving.

Absolute Max Rating

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5 ①	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.1①	
I_{DM}	Pulsed Drain Current ②	15	
$P_D @ TC = 25^\circ C$	Power Dissipation ③	50	W
	Linear Derating Factor	0.4	W/°C
V_{DS}	Drain-Source Voltage	650	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=22.4mH	54	mJ
I_{AR}	Avalanche Current @ L=22.4mH	2.2	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

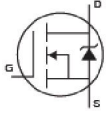
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	2.5	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	—	75	$^{\circ}C/W$

Electrical Characteristics @ $T_A=25^{\circ}C$ unless otherwise specified

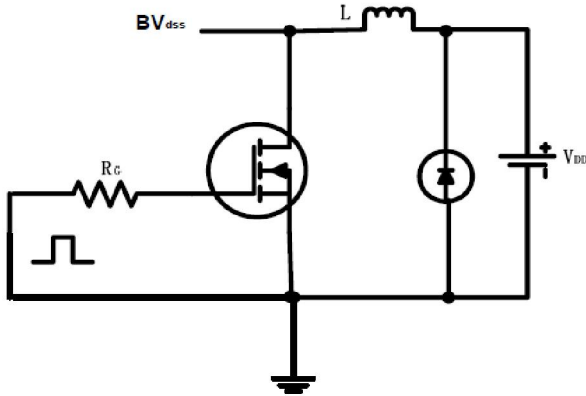
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	650	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	1.0	1.2	Ω	$V_{GS}=10V, I_D = 1A$ $T_J = 125^{\circ}C$
		—	2.2	—		
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$ $T_J = 125^{\circ}C$
		—	2.7	—		
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	$V_{DS} = 650V, V_{GS} = 0V$ $T_J = 125^{\circ}C$
		—	—	50		
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 30V$
		—	—	-100		$V_{GS} = -30V$
Q_g	Total gate charge	—	8.3	—	nC	$I_D = 4A,$ $V_{DS}=100V,$ $V_{GS} = 10V$
Q_{gs}	Gate-to-Source charge	—	2.3	—		
Q_{gd}	Gate-to-Drain("Miller") charge	—	2.6	—		
$t_{d(on)}$	Turn-on delay time	—	9.9	—	ns	$V_{GS}=10V, V_{DS}=380V,$ $R_{GEN}=18\Omega, I_D=4.5A$
t_r	Rise time	—	18.4	—		
$t_{d(off)}$	Turn-Off delay time	—	18.1	—		
t_f	Fall time	—	15.3	—		
C_{iss}	Input capacitance	—	267	—	pF	$V_{GS} = 0V$
C_{oss}	Output capacitance	—	220	—		$V_{DS} = 25V$
C_{rss}	Reverse transfer capacitance	—	4.76	—		$f = 1MHz$

Source-Drain Ratings and Characteristics

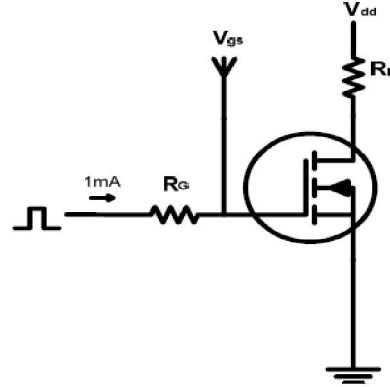
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	15	A	
V_{SD}	Diode Forward Voltage	—	0.85	1.2	V	$I_S=2.8A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	—	284	—	nS	$T_J = 25^{\circ}C, I_F = I_S,$
Q_{rr}	Reverse Recovery Charge	—	1395	—	nC	$di/dt = 100A/\mu s$

Test Circuits and Waveforms

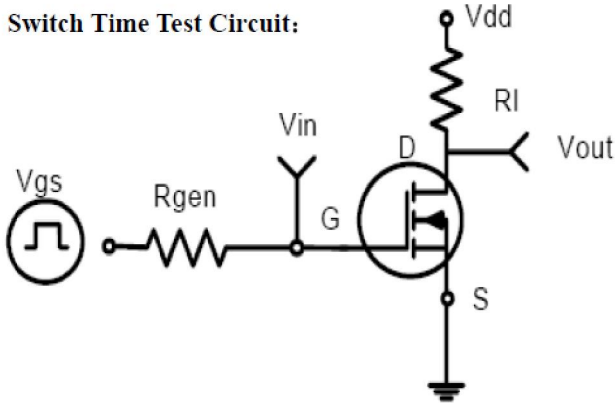
EAS test circuits:



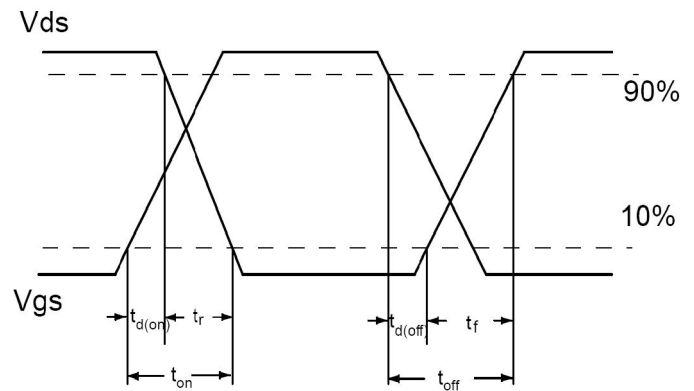
Gate charge test circuit:



Switch Time Test Circuit:



Waveforms:



Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$

Typical Electrical and Thermal Characteristics

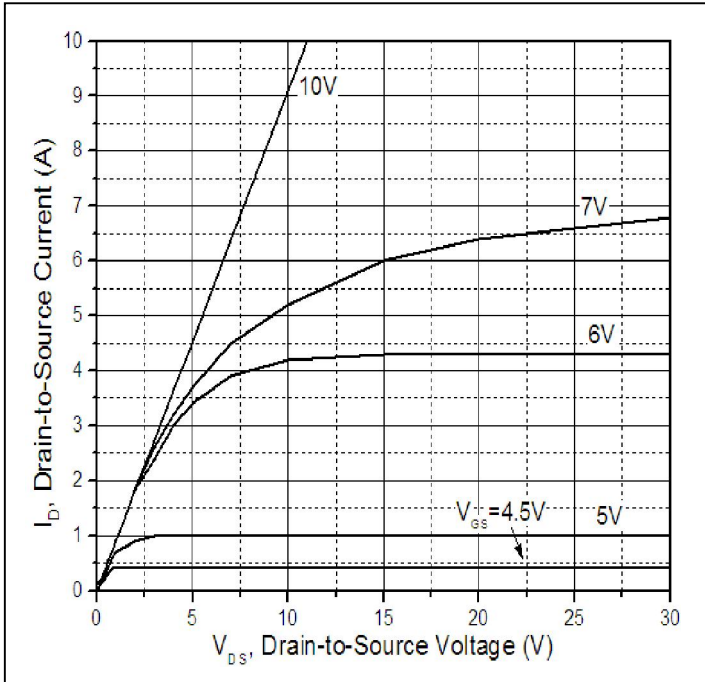


Figure 1: Typical Output Characteristics

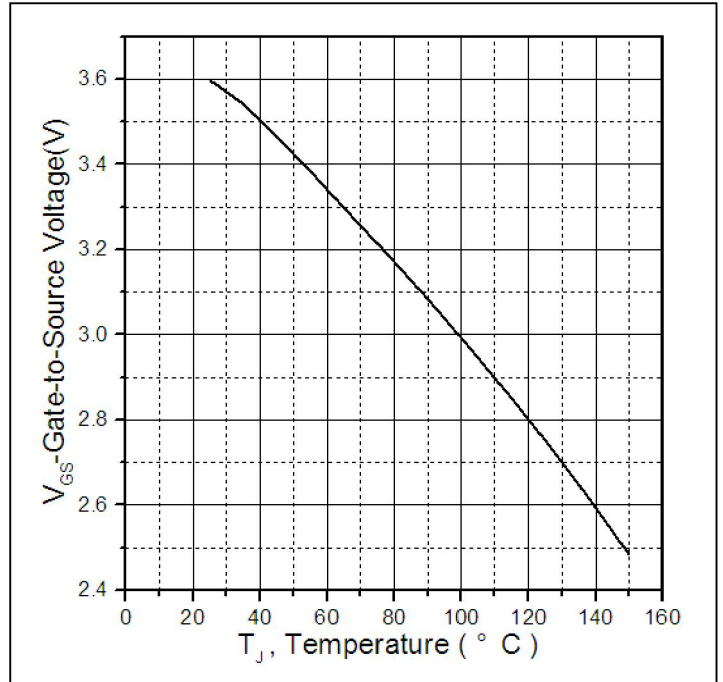


Figure 2: Gate to source cut-off voltage

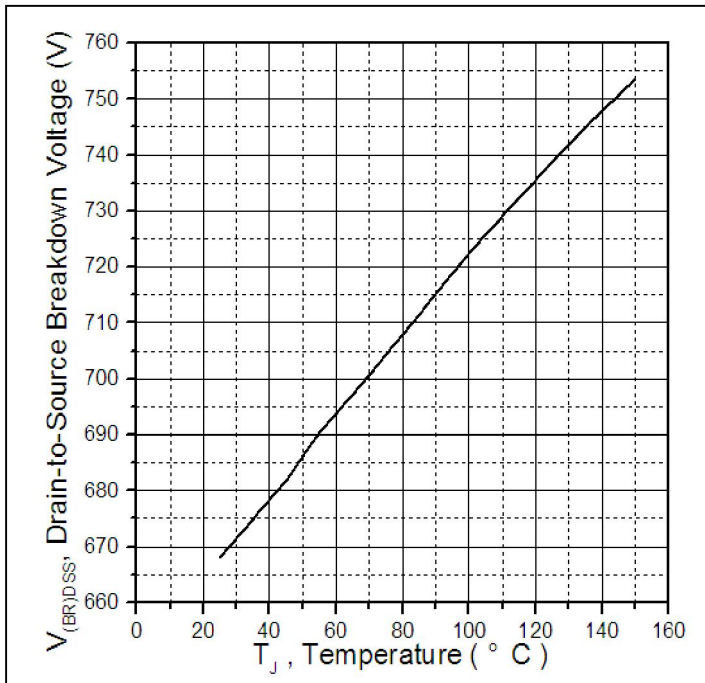


Figure 3: Drain-to-Source Breakdown Voltage Vs. Case Temperature

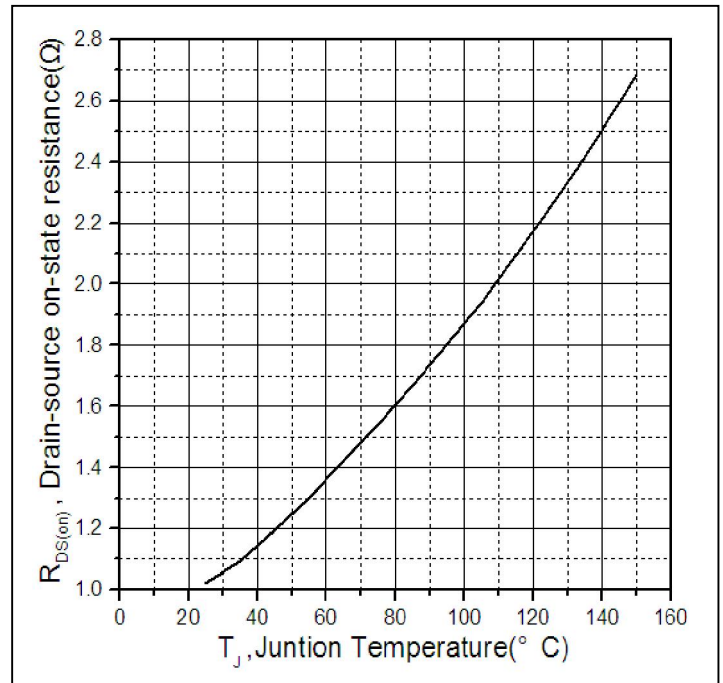


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical Electrical and Thermal Characteristics

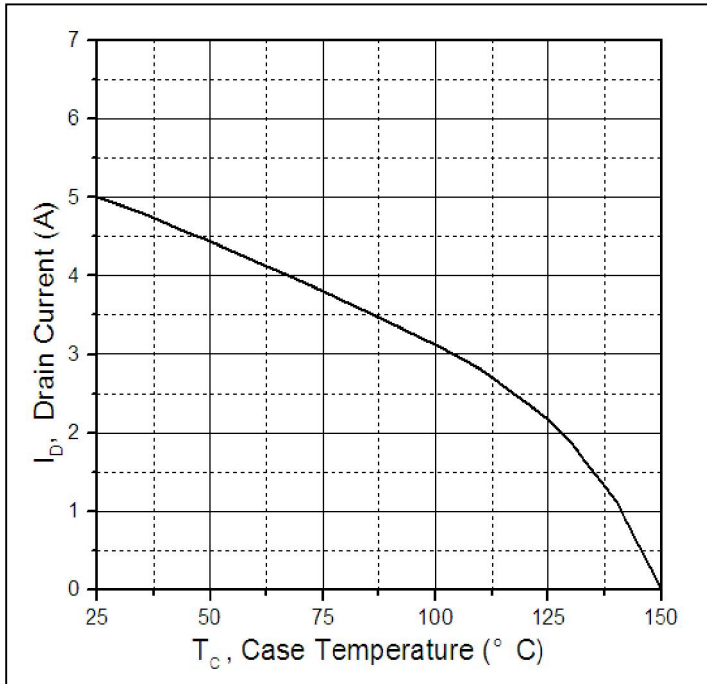


Figure 5. Maximum Drain Current Vs. Case Temperature

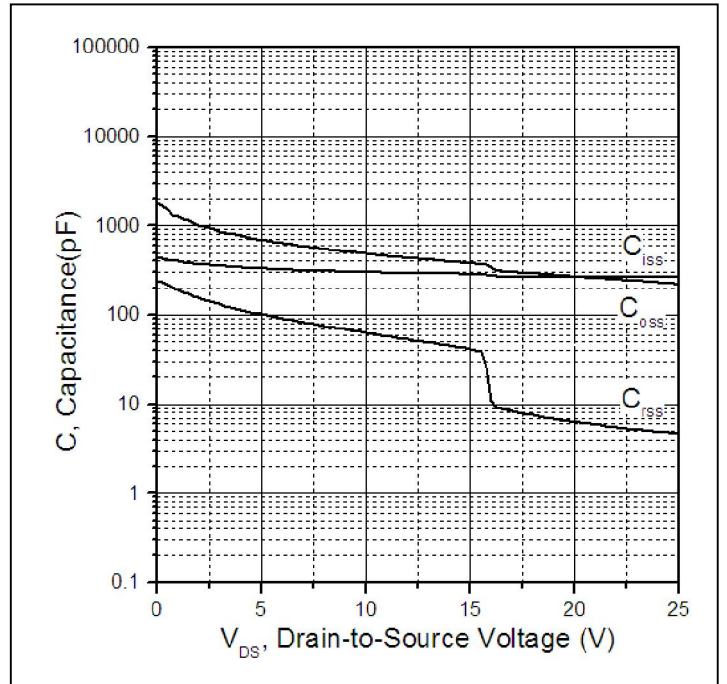


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

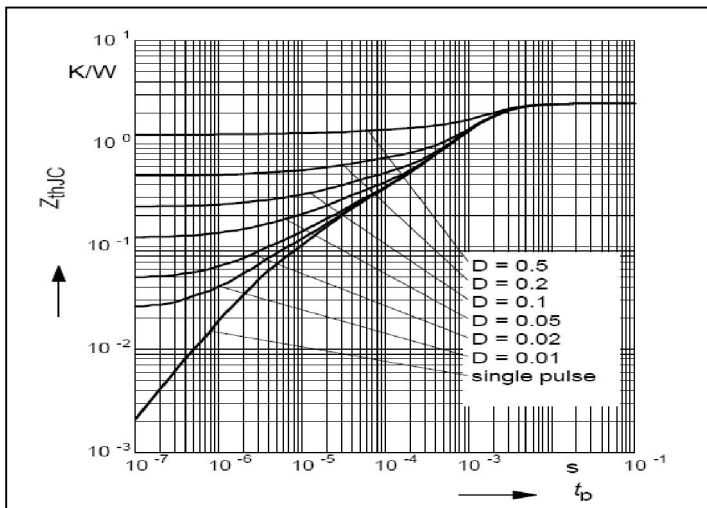
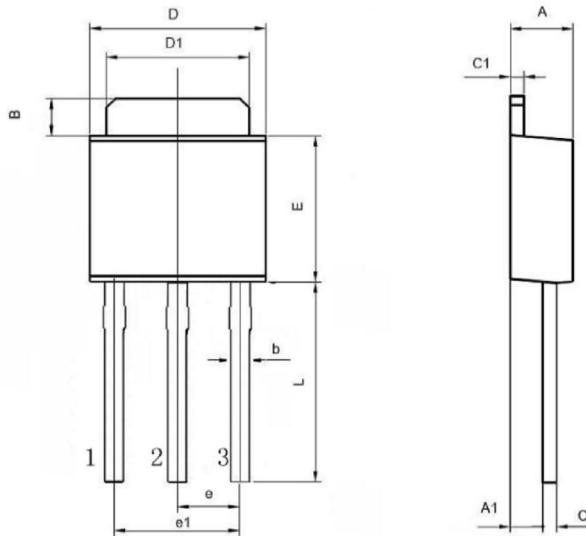


Figure 7. Maximum Effective Transient Thermal Impedance Junction-to-Case

Mechanical Data

TO-251 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	-	2.400	0.087	-	0.094
A1	0.950	-	1.150	0.037	-	0.045
B	0.950	-	1.250	0.037	-	0.049
b	0.500	-	0.700	0.020	-	0.028
c	0.450	-	0.550	0.018	-	0.022
c1	0.450	-	0.550	0.018	-	0.022
D	6.450	-	6.750	0.254	-	0.266
D1	5.200	-	5.400	0.205	-	0.213
E	5.950	-	6.250	0.234	-	0.246
e	2.240	-	2.340	0.088	-	0.092
e1	4.430	-	4.730	0.174	-	0.186
L	9.000	-	9.400	0.354	-	0.370



Ordering and Marking Information

Device Marking: SSF5NS65G

Package (Available)
TO-251(IPAK)
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-251	80	60	4800	5	24000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices