

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# RQK0601AGDQS

Silicon N Channel MOS FET  
Power Switching

REJ03G0575-0400

Rev.4.00

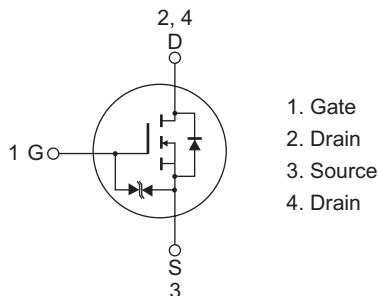
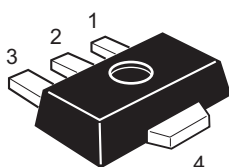
Jun 22, 2006

## Features

- Low on-resistance  
 $R_{DS(on)} = 56 \text{ m}\Omega$  typ ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 2.5 \text{ A}$ )
- Low drive current
- High speed switching
- 4.5 V gate drive

## Outline

RENESAS package code: PLZZ0004CA-A  
(Package name: UPAK®)



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "AG".

\*UPAK is a trademark of Renesas Technology Corp.

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	5	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	7.3	A
Body - drain diode reverse drain current	$I_{DR}$	5	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	1.5	W
Channel dissipation	$P_{ch(pulse)}$ <sup>Note1</sup>	5	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 1 \text{ s}$ , duty cycle  $\leq 1\%$

2. When using the glass epoxy board (FR-4: 40 x 40 x 1 mm)

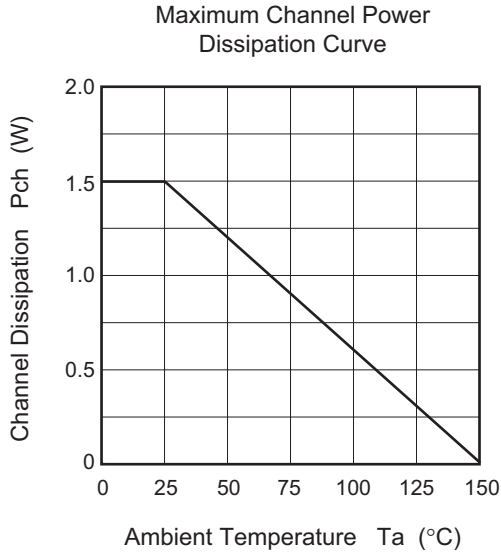
## Electrical Characteristics

(Ta = 25°C)

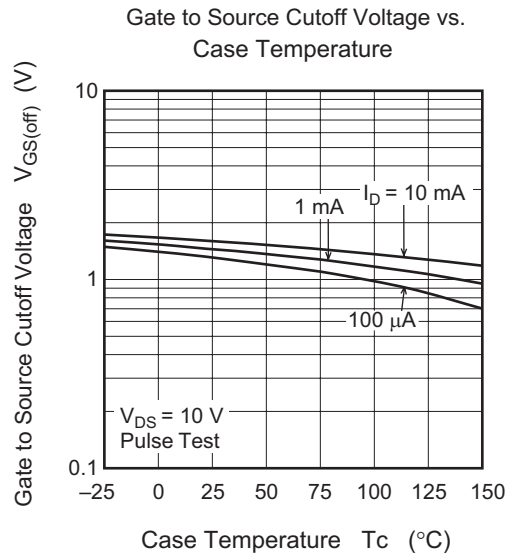
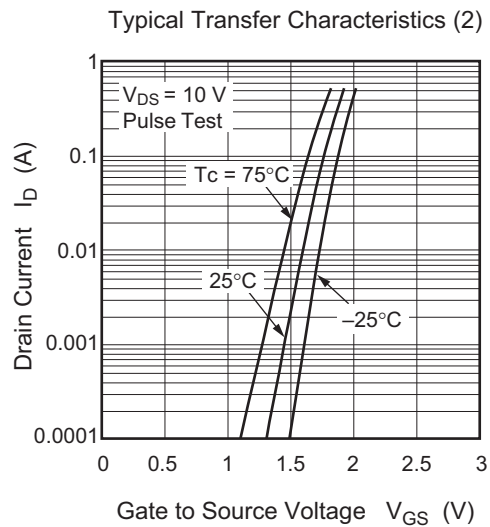
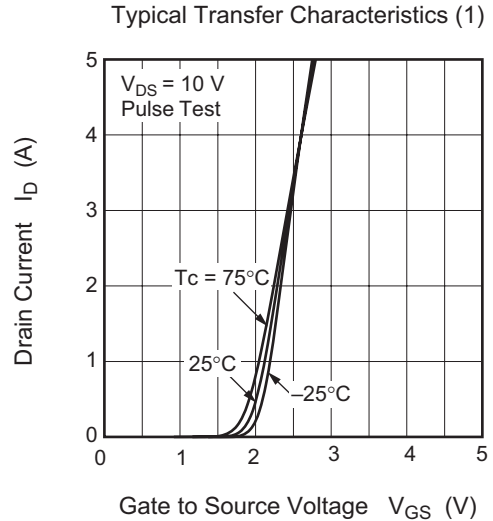
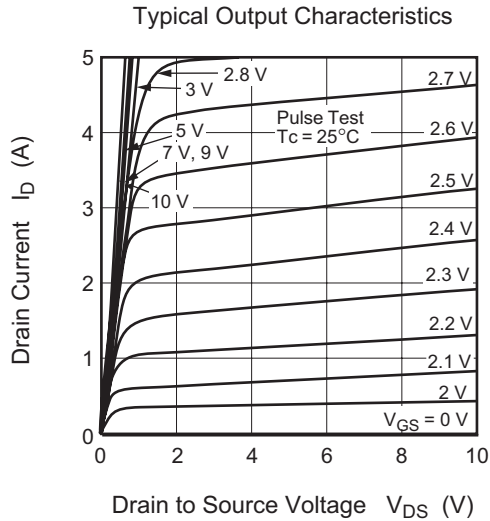
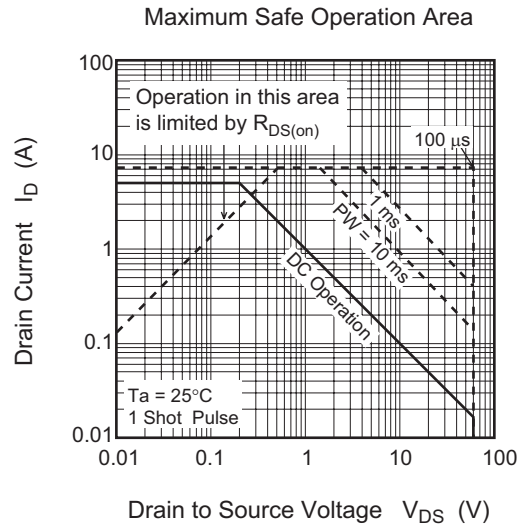
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \mu\text{A}, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$
Drain to source leak current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	56	70	m $\Omega$	$I_D = 2.5 \text{ A}, V_{GS} = 10 \text{ V}^{\text{Note3}}$
	$R_{DS(on)}$	—	65	91	m $\Omega$	$I_D = 2.5 \text{ A}, V_{GS} = 4.5 \text{ V}^{\text{Note3}}$
Forward transfer admittance	$ y_{fs} $	5.2	8.7	—	S	$I_D = 2.5 \text{ A}, V_{DS} = 10 \text{ V}^{\text{Note3}}$
Input capacitance	$C_{iss}$	—	540	—	pF	$V_{DS} = 10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	75	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	29	—	pF	
Turn - on delay time	$t_{d(on)}$	—	11	—	ns	$I_D = 1 \text{ A}, V_{GS} = 10 \text{ V},$ $R_L = 10 \Omega, R_g = 4.7 \Omega$
Rise time	$t_r$	—	38	—	ns	
Turn - off delay time	$t_{d(off)}$	—	49	—	ns	
Fall time	$t_f$	—	3.1	—	ns	
Total gate charge	$Q_g$	—	8.9	—	nC	$V_{DD} = 10 \text{ V}, V_{GS} = 10 \text{ V},$ $I_D = 5 \text{ A}$
Gate to source charge	$Q_{gs}$	—	1.3	—	nC	
Gate to drain charge	$Q_{gd}$	—	1.0	—	nC	
Body - drain diode forward voltage	$V_{DF}$	—	0.8	—	V	$I_F = 1.5 \text{ A}, V_{GS} = 0^{\text{Note3}}$

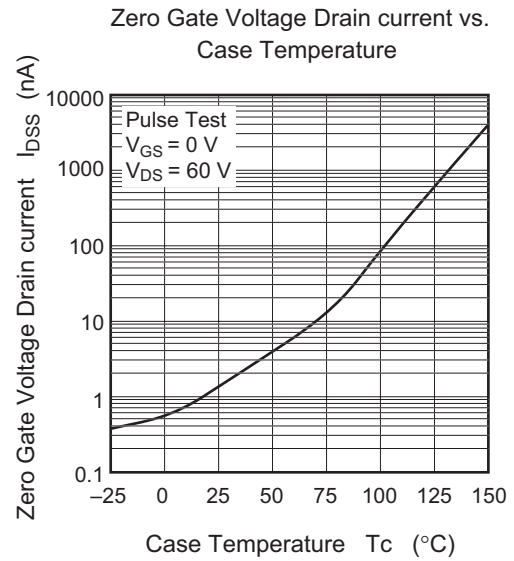
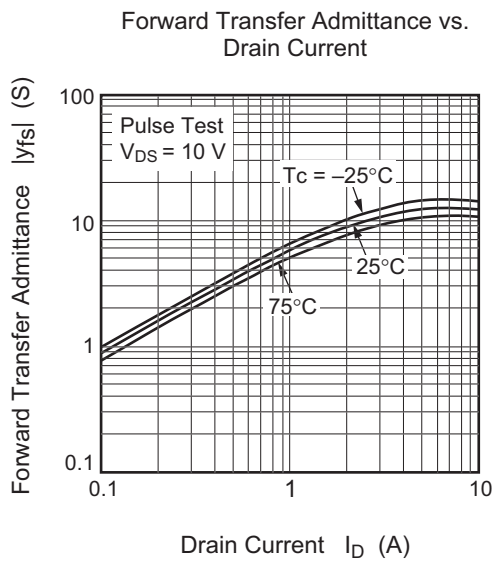
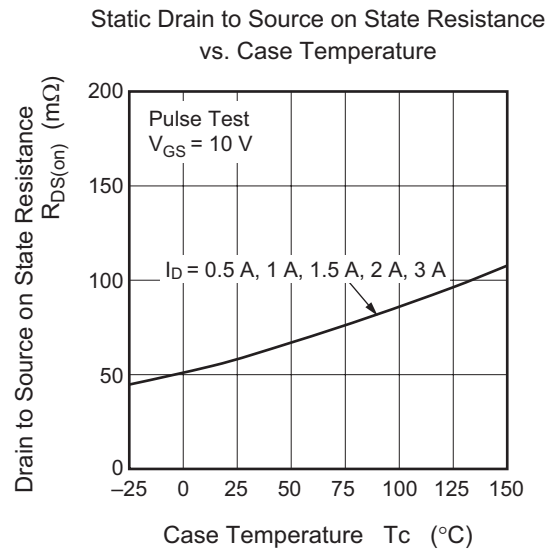
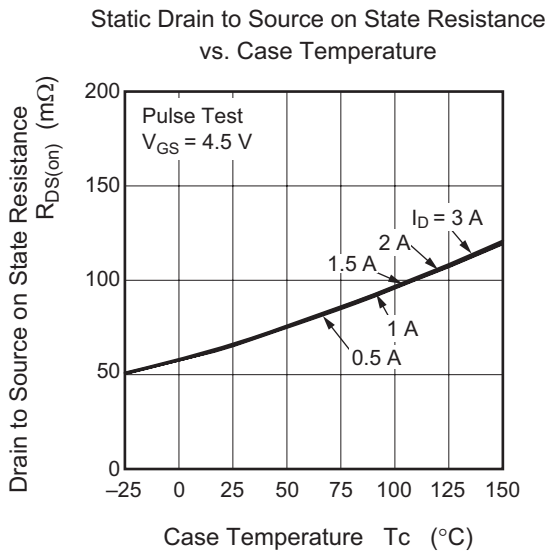
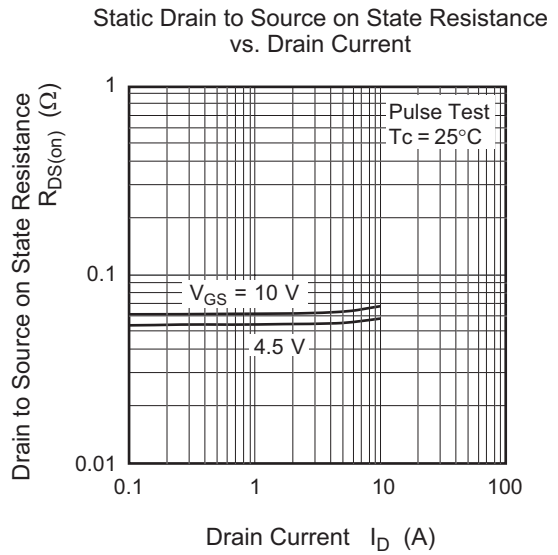
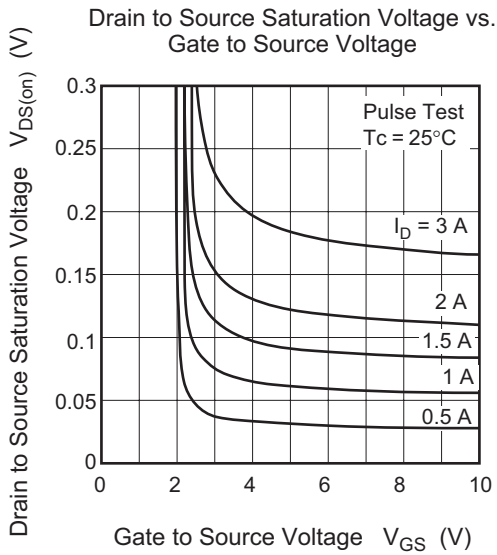
Notes: 3. Pulse test

Main Characteristics

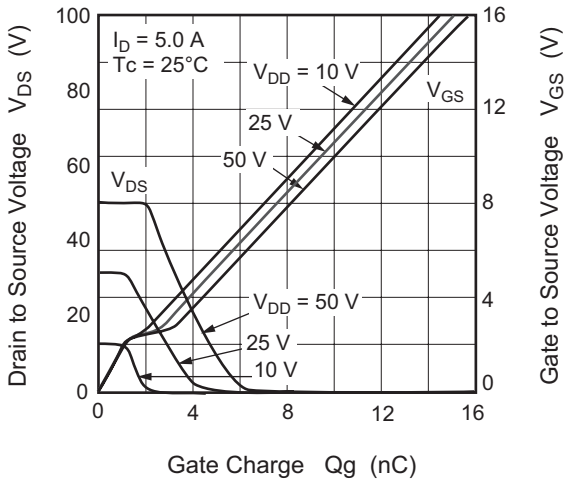


\*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

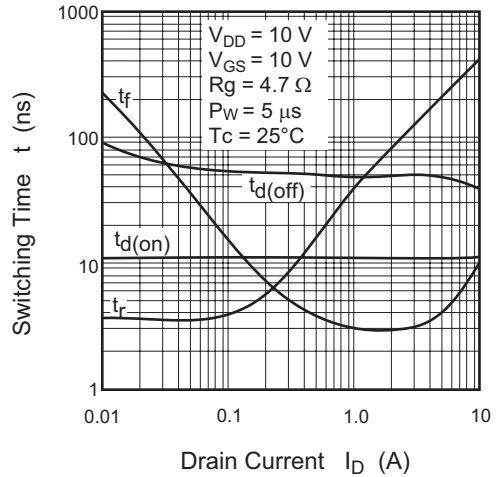




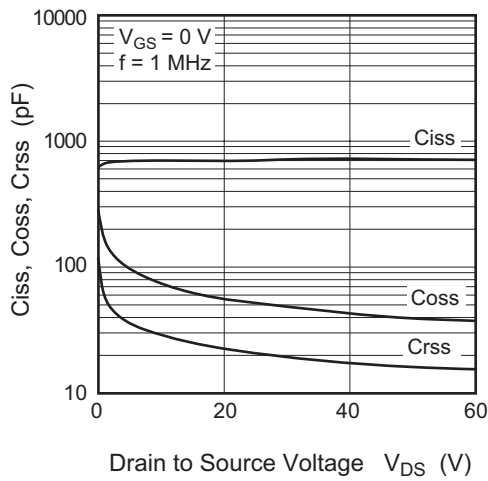
Dynamic Input Characteristics



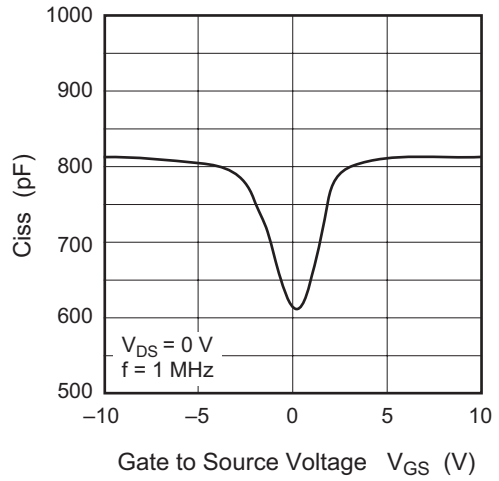
Switching Characteristics



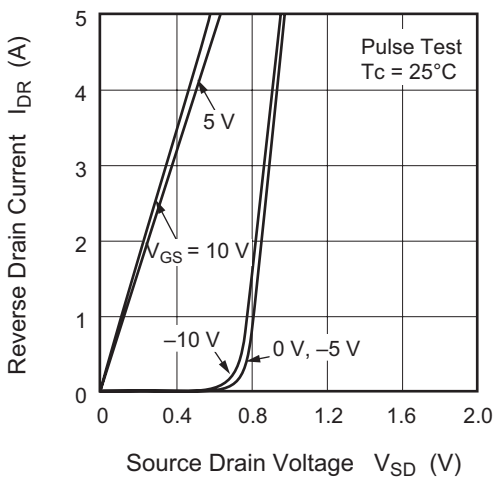
Typical Capacitance vs. Drain to Source Voltage



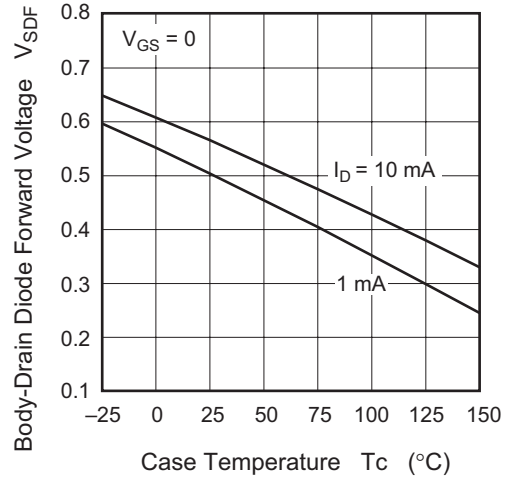
Input Capacitance vs. Gate to Source Voltage



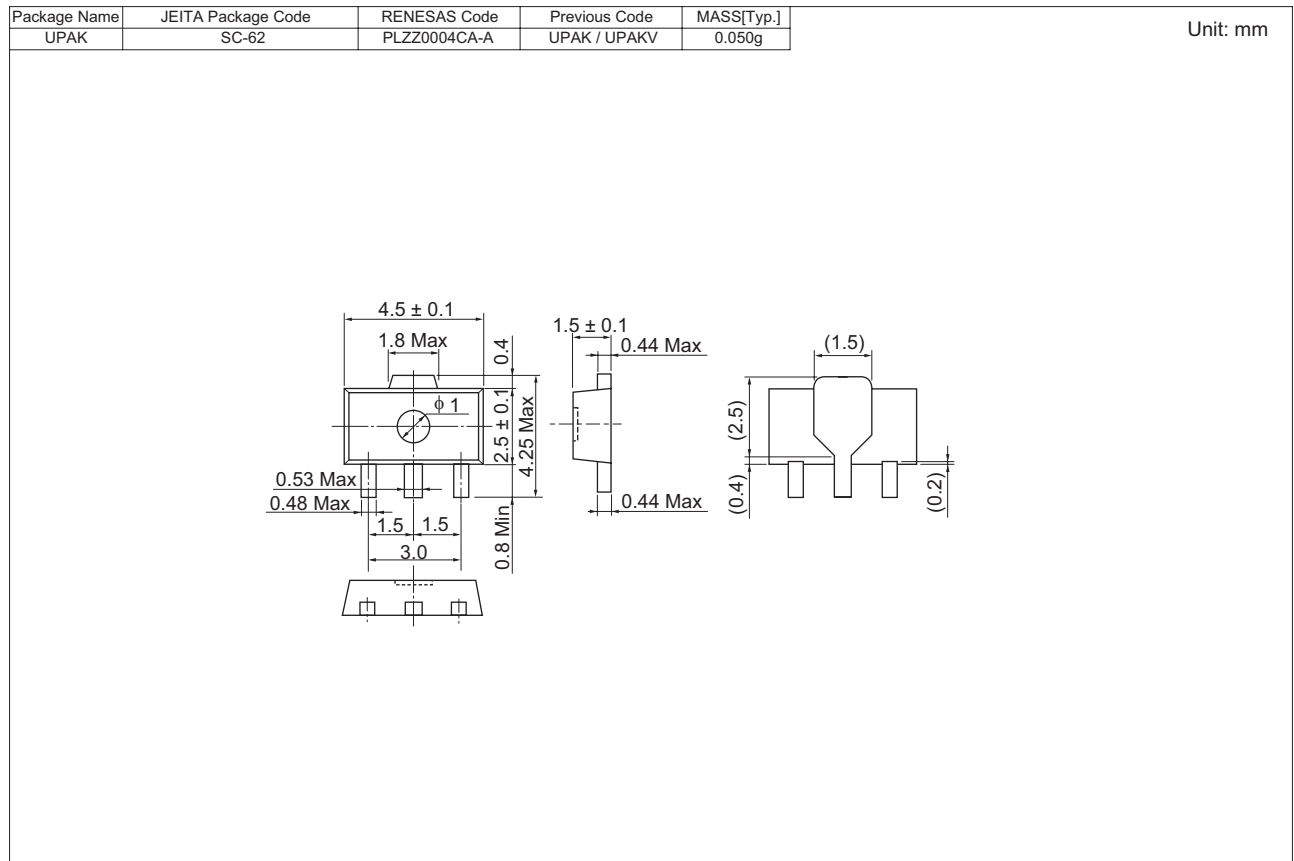
Reverse Drain Current vs. Source to Drain Voltage



Body-Drain Diode Forward Voltage vs. Case Temperature



### Package Dimensions



### Ordering Information

Part Name	Quantity	Shipping Container
RQK0601AGDQSTL-E	1000 pcs.	$\phi 178$ reel, 12 mm Emboss taping



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**Renesas Technology America, Inc.**

450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**

Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

**Renesas Technology Hong Kong Ltd.**

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**

10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology Singapore Pte. Ltd.**

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510