

RJK0216DPA

Silicon N Channel Power MOS FET with Schottky Barrier Diode High Speed Power Switching

R07DS0208EJ0110

Rev.1.10

Sep 05, 2011

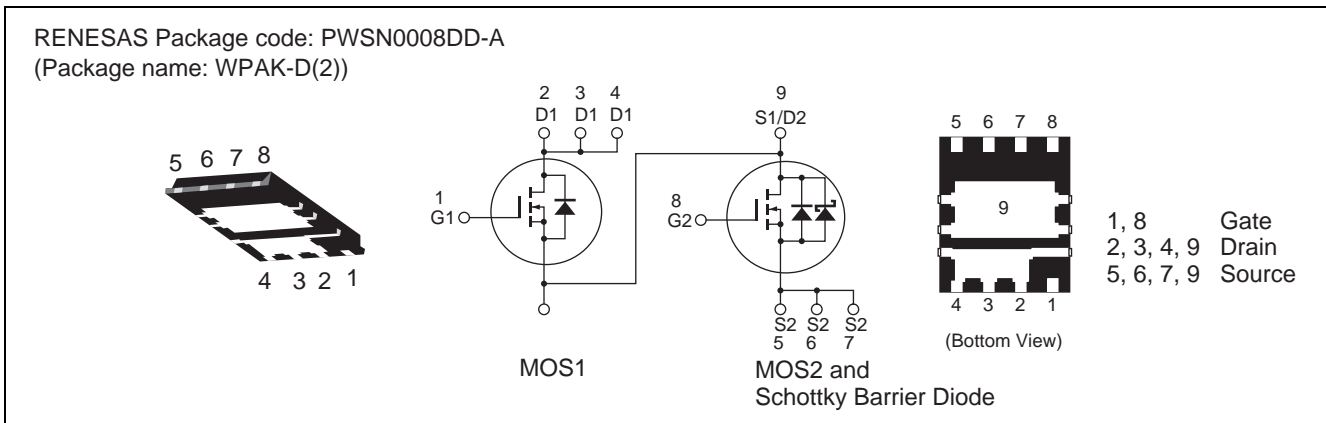
Applications

DC-DC conversion for PC and Server.

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Pb-free
- Halogen-free

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2	
Drain to source voltage	V _{DSS}	25	25	V
Gate to source voltage	V _{GS}	±20	±20	V
Drain current	I _D	15	32	A
Drain peak current	I _{D(pulse)} ^{Note1}	60	128	A
Reverse drain current	I _{DR}	15	32	A
Avalanche current	I _{AP} ^{Note 2}	5	10	A
Avalanche energy	E _{AR} ^{Note 2}	3.1	12.5	mJ
Channel dissipation	P _{ch} ^{Note3}	10	20	W
Channel temperature	T _{ch}	150	150	°C
Storage temperature	T _{stg}	-55 to +150	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
 2. Value at T_{ch} = 25°C, R_g ≥ 50 Ω
 3. T_c=25°C

Electrical Characteristics

• MOS1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	25	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 25 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	7.6	9.2	$\text{m}\Omega$	$I_D = 7.5 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	10.5	13.7	$\text{m}\Omega$	$I_D = 7.5 \text{ A}, V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	30	—	S	$I_D = 7.5 \text{ A}, V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	810	1130	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	130	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	74	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.2	2.4	Ω	
Total gate charge	Q_g	—	6.2	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	2.8	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	1.9	—	nC	$I_D = 15 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	7.3	—	ns	$V_{GS} = 10 \text{ V}, I_D = 7.5 \text{ A}$
Rise time	t_r	—	5.3	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	33.9	—	ns	$R_L = 1.33 \Omega$
Fall time	t_f	—	5.4	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.84	1.10	V	$I_F = 15 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	20	—	ns	$I_F = 15 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

• MOS2

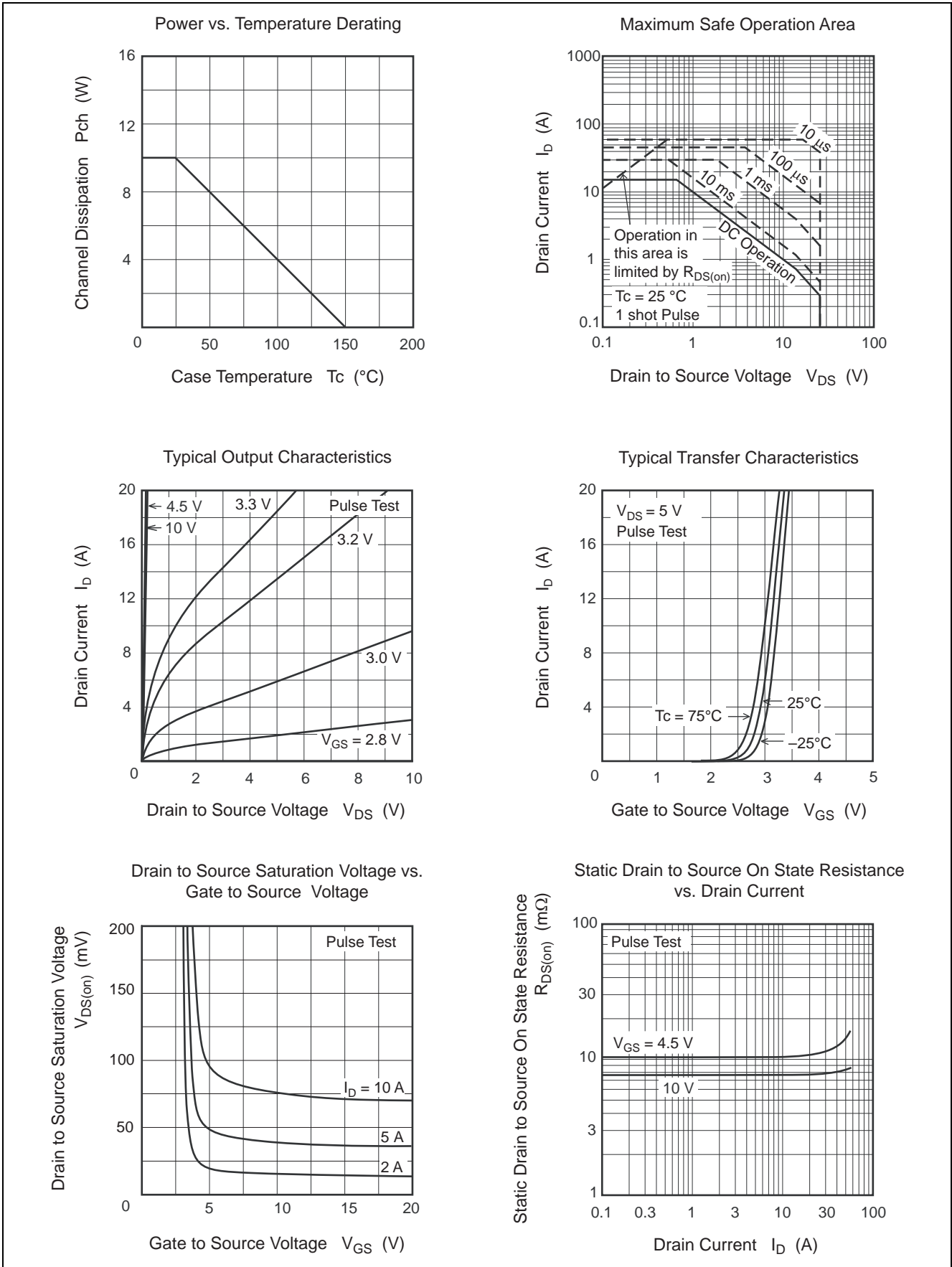
(Ta = 25°C)

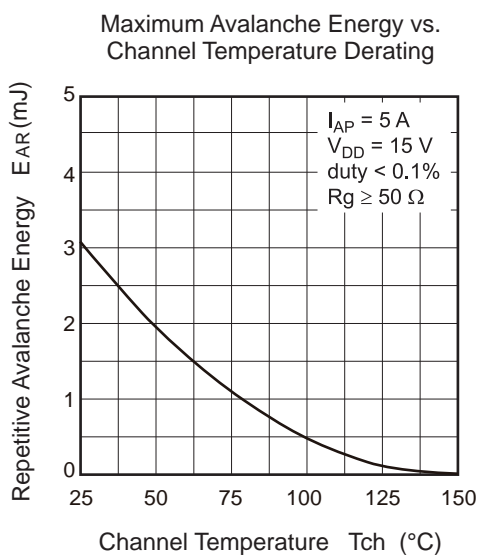
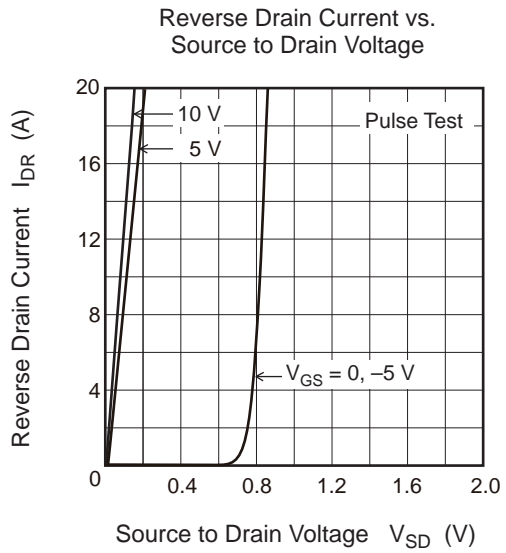
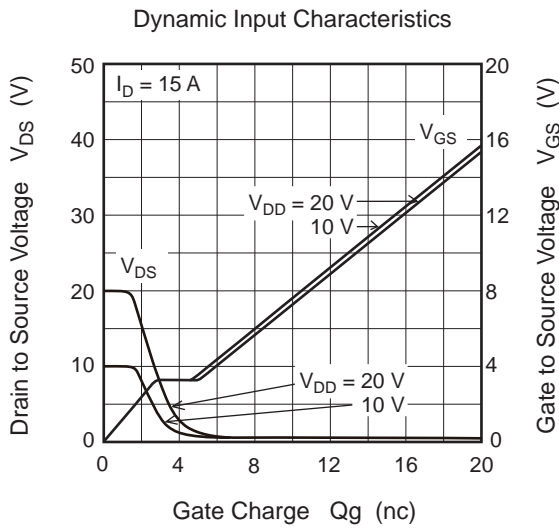
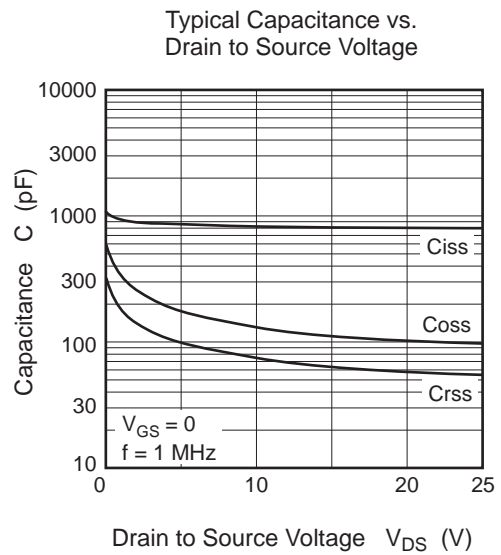
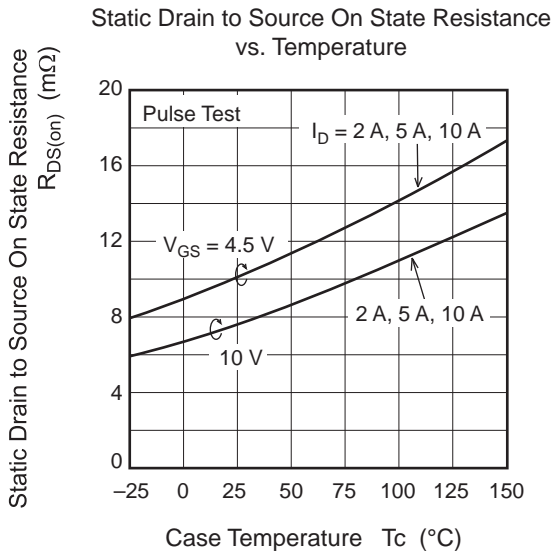
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	25	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	mA	$V_{DS} = 25 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.6	4.4	m Ω	$I_D = 16 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	5.7	7.4	m Ω	$I_D = 16 \text{ A}, V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	50	—	S	$I_D = 16 \text{ A}, V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1600	2240	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	310	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	170	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.7	3.4	Ω	
Total gate charge	Q_g	—	11.6	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	5.1	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	3.6	—	nC	$I_D = 32 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	9.6	—	ns	$V_{GS} = 10 \text{ V}, I_D = 16 \text{ A}$
Rise time	t_r	—	5.3	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	38.9	—	ns	$R_L = 0.63 \Omega$
Fall time	t_f	—	5.9	—	ns	$R_g = 4.7 \Omega$
Schottky Barrier diode forward voltage	V_F	—	0.39	—	V	$I_F = 2 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	20	—	ns	$I_F = 32 \text{ A}, V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse

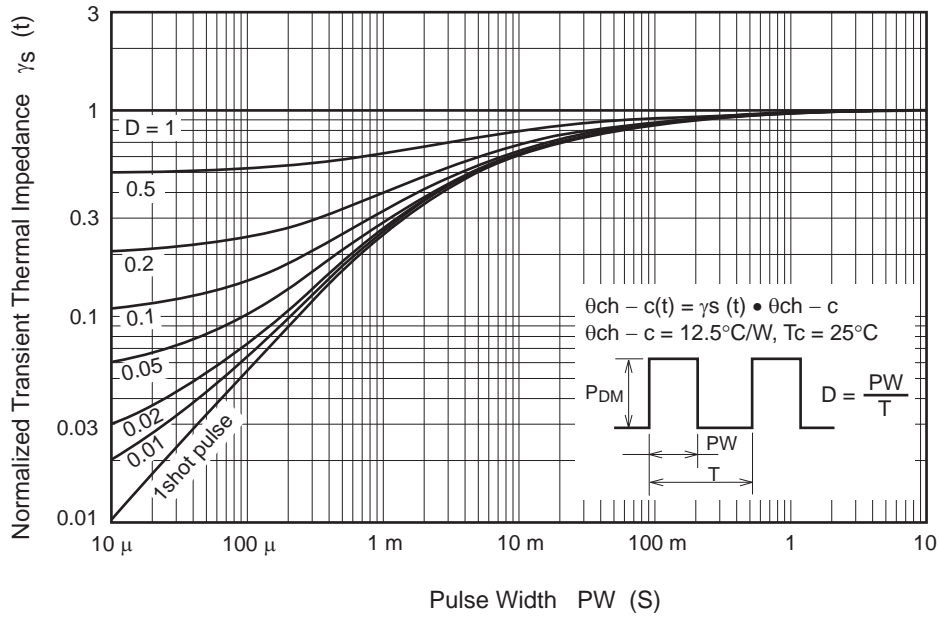
Main Characteristics

• MOS1

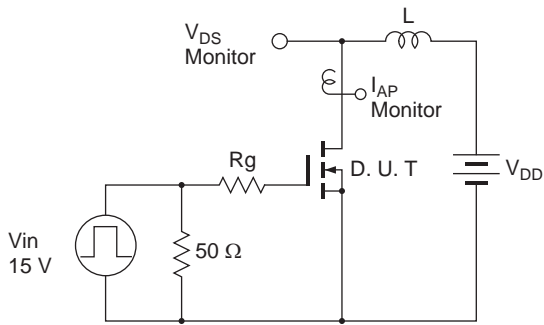




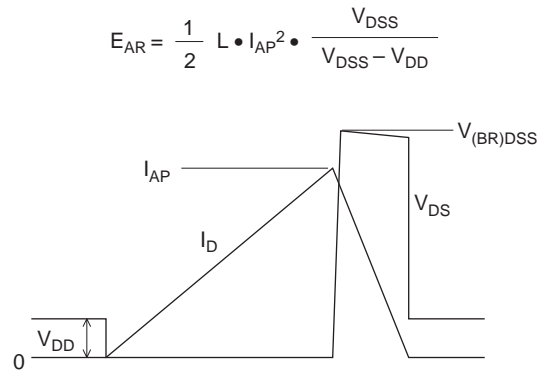
Normalized Transient Thermal Impedance vs. Pulse Width



Avalanche Test Circuit

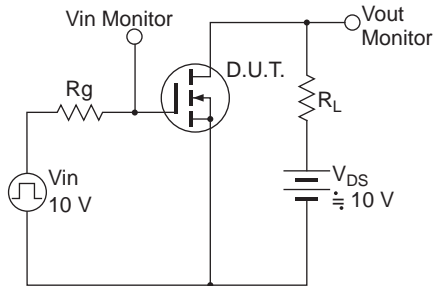


Avalanche Waveform

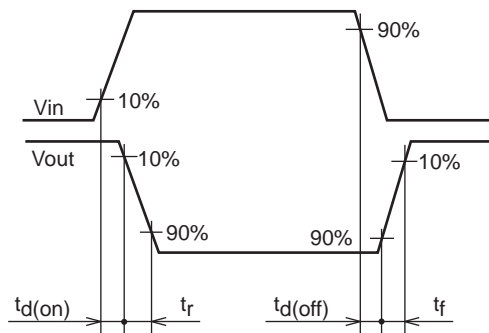


$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

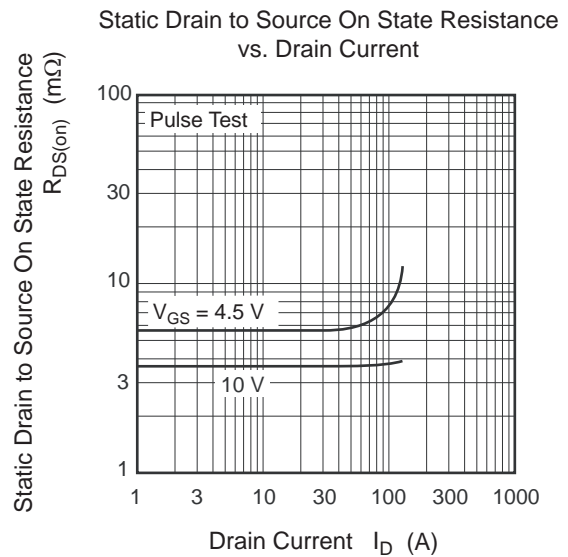
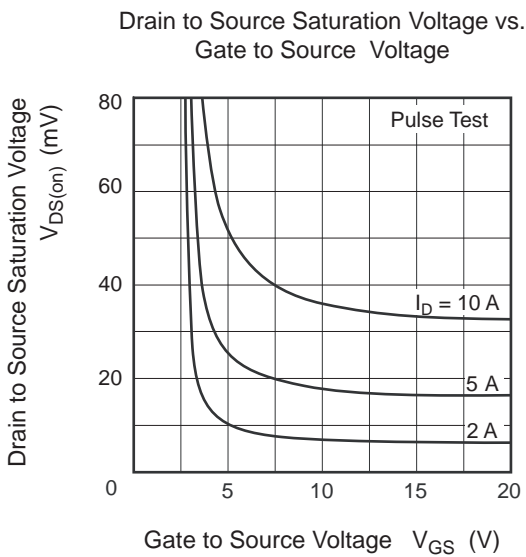
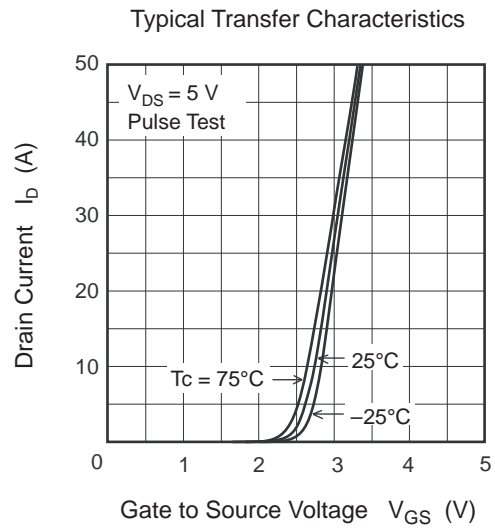
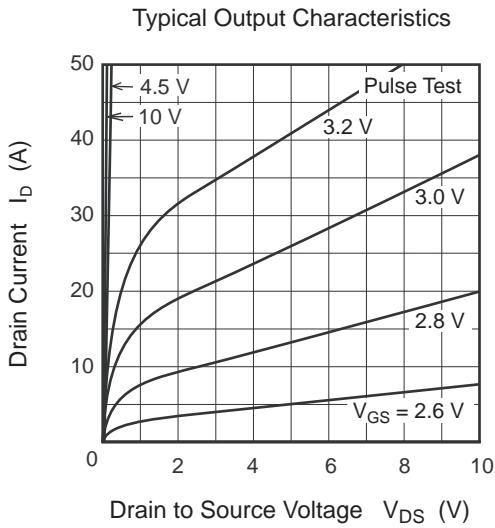
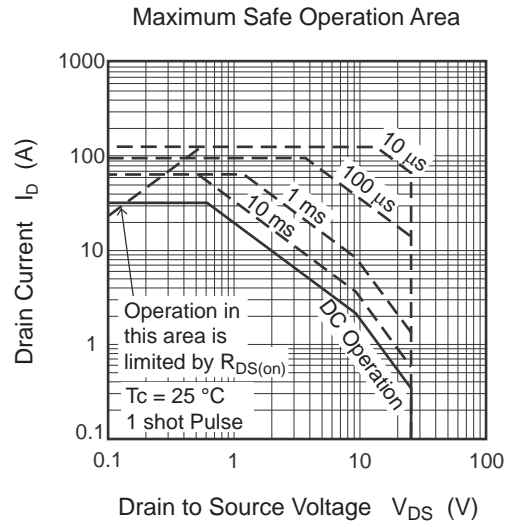
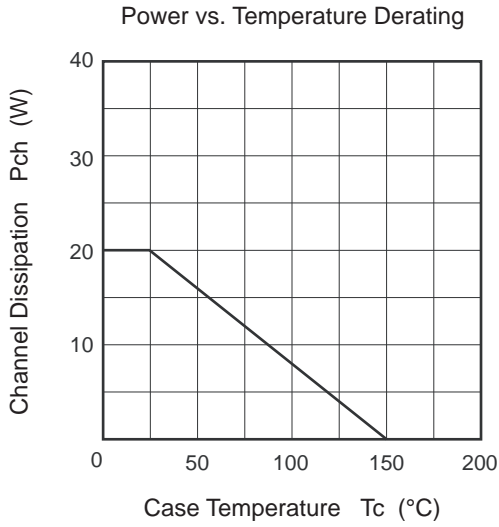
Switching Time Test Circuit

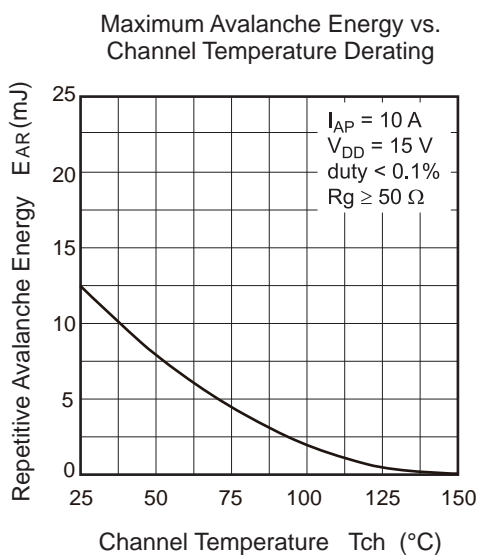
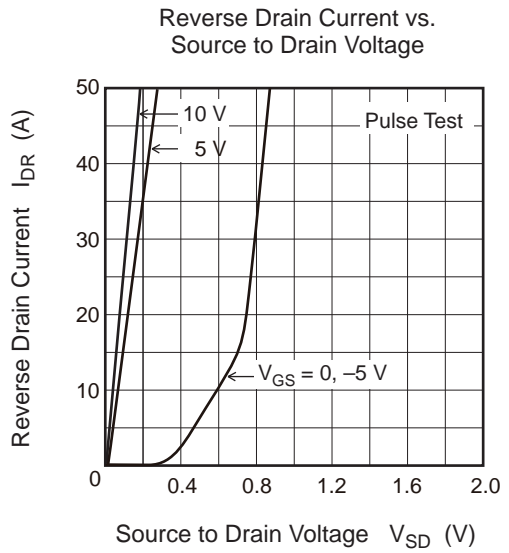
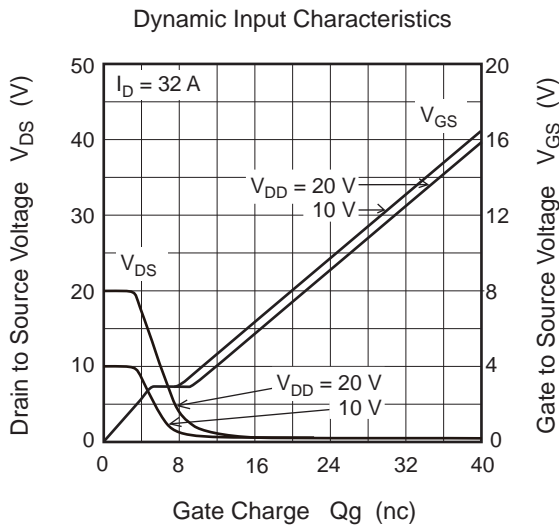
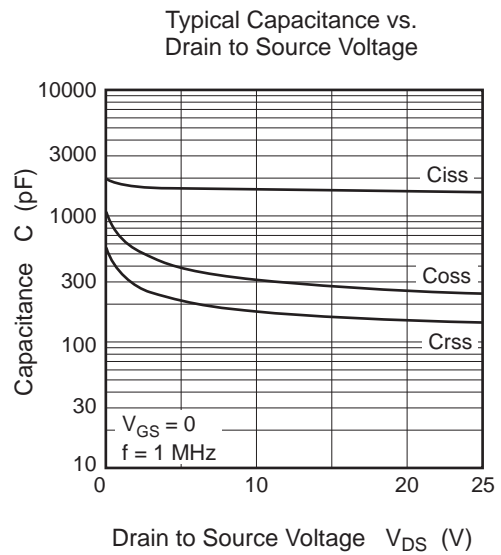
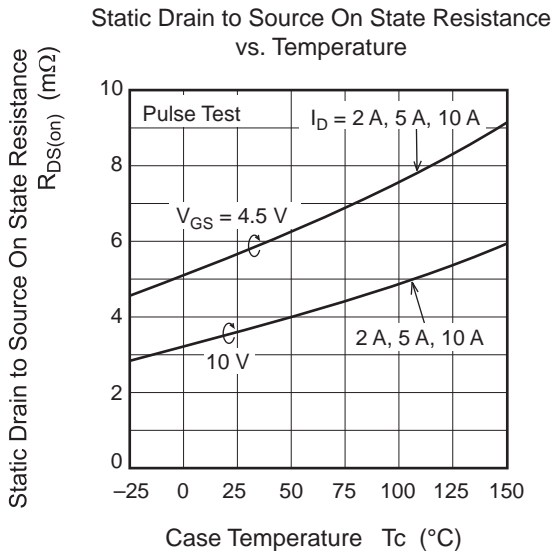


Switching Time Waveform

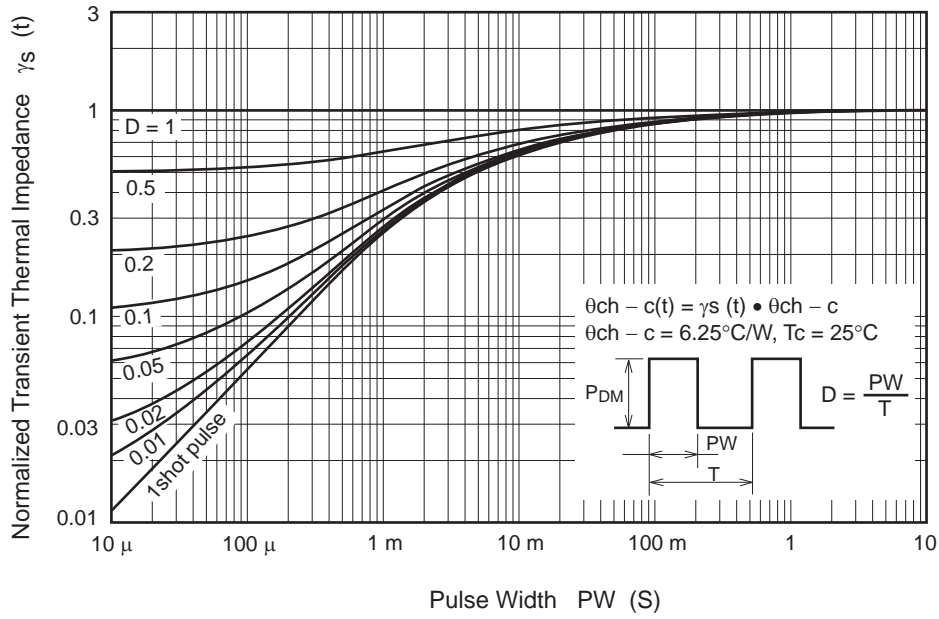


• MOS2 and Schottky Barrier Diode

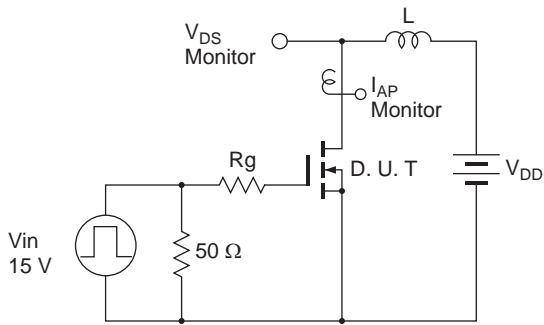




Normalized Transient Thermal Impedance vs. Pulse Width

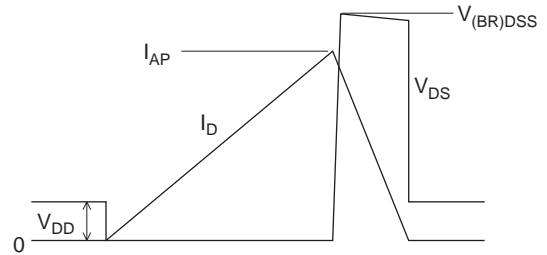


Avalanche Test Circuit

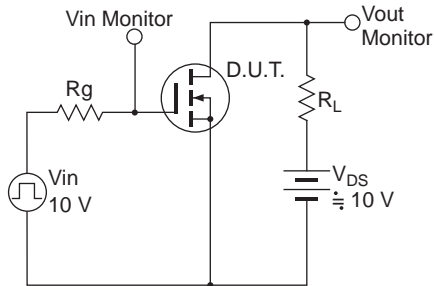


Avalanche Waveform

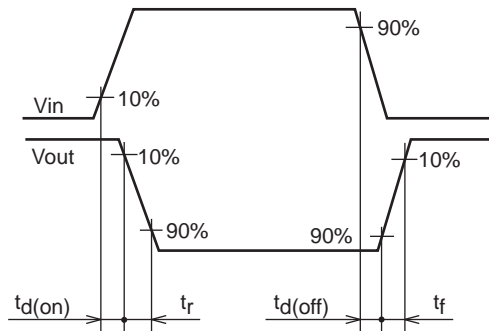
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



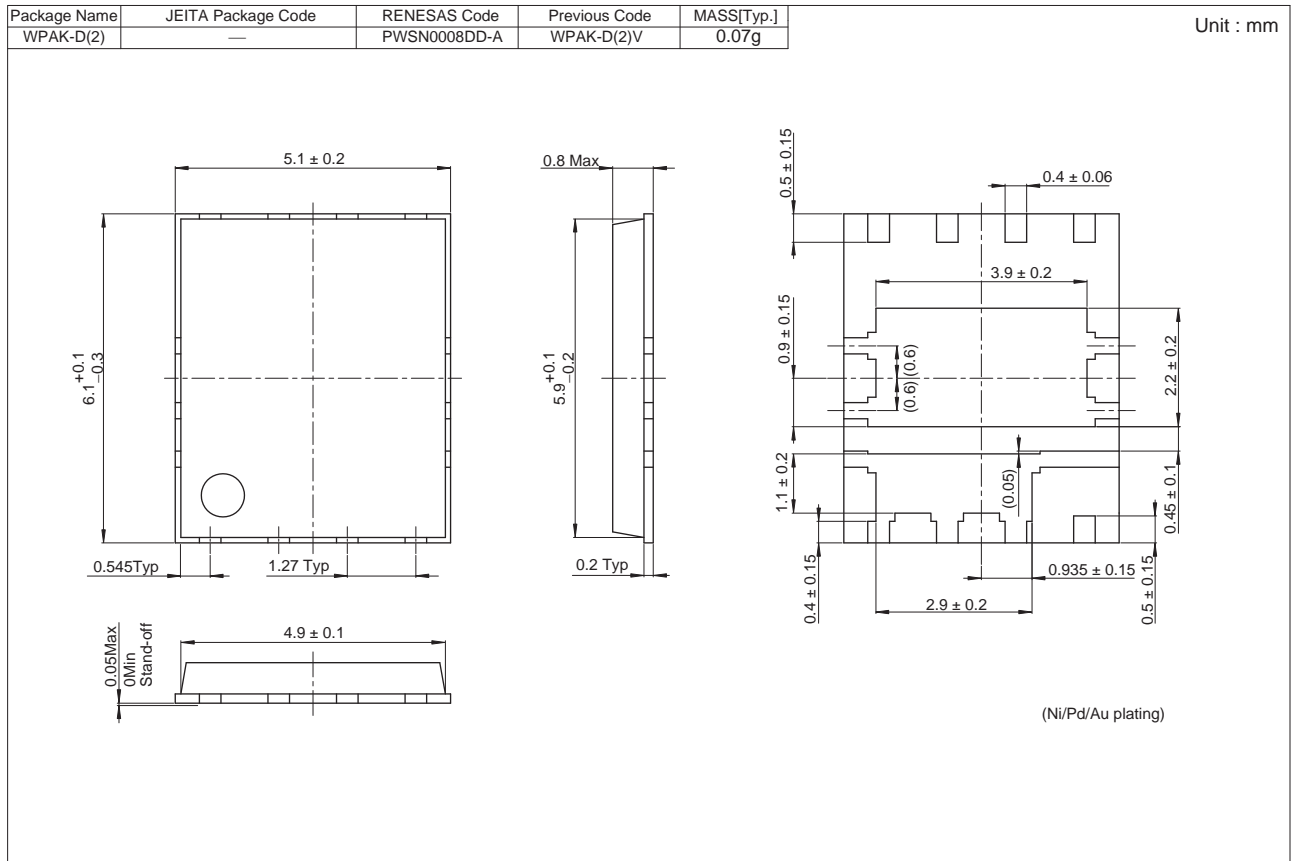
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK0216DPA-00-J53	3000 pcs	Taping

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Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
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