FAIRCHILD SEMICONDUCTOR TM

RFL1N10L

1A, 100V, 1.200 Ohm, Logic Level, N-Channel Power MOSFET

August 1999

Features

- **1A, 100V**
- **$r_{DS(ON)}$ = 1.200Ω**

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFL1N10L	TO-205AF	RFL1N10L

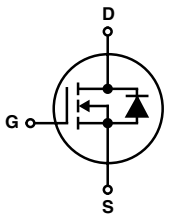
NOTE: When ordering, use the entire part number.

Description

This is an N-Channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

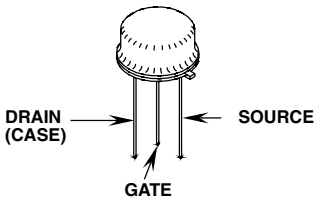
Formerly developmental type TA09524.

Symbol



Packaging

JEDEC TO-205AF



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFL1N10L	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	100	V
Drain to Gate Voltage (R_{GS} = 1MΩ) (Note 1)	V_{DGR}	100	V
Continuous Drain Current	I_D	1	A
Pulsed Drain Current (Note 3)	I_{DM}	5	A
Gate to Source Voltage	V_{GS}	±10	V
Maximum Power Dissipation	P_D	8.33	W
Above $T_C = 25^oC$, Derate Linearly		0.0667	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0	100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA	1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}	-	-	1	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{DS} = 80V, $T_C = 125^oC$	-	-	25	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 1A, V_{GS} = 5V (Figures 6, 7)	-	-	1.200	Ω
Drain to Source On Voltage (Note 2)	$V_{DS(ON)}$	I_D = 1A, V_{GS} = 5V	-	-	1.2	V
Turn-On Delay Time	$t_{d(ON)}$	$I_D \approx$ 1A, V_{DD} = 50V, R_G = 6.25Ω, V_{GS} = 5V, R_L = 50Ω (Figures 10, 11, 12)	-	10	25	ns
Rise Time	t_r		-	15	45	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	25	45	ns
Fall Time	t_f		-	30	50	ns
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz (Figure 9)	-	-	200	pF
Output Capacitance	C_{OSS}		-	-	80	pF
Reverse Transfer Capacitance	C_{RSS}		-	-	35	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	15	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 1A	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 2A, dI_{SD}/dt = 50A/μs	-	100	-	ns

NOTES:

2. Pulse test: width ≤ 300μs duty cycle ≤ 2%.
3. Repetitive rating: pulse witdh limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

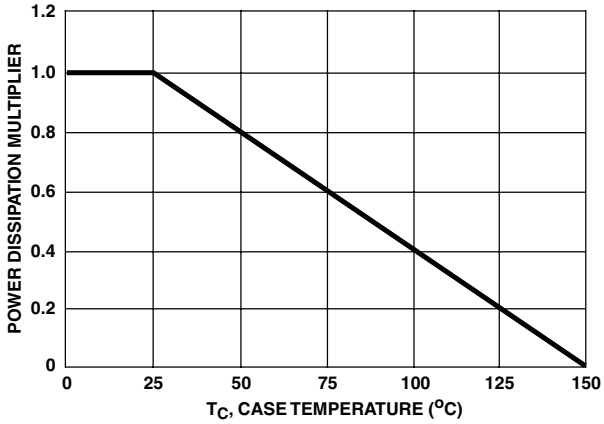


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

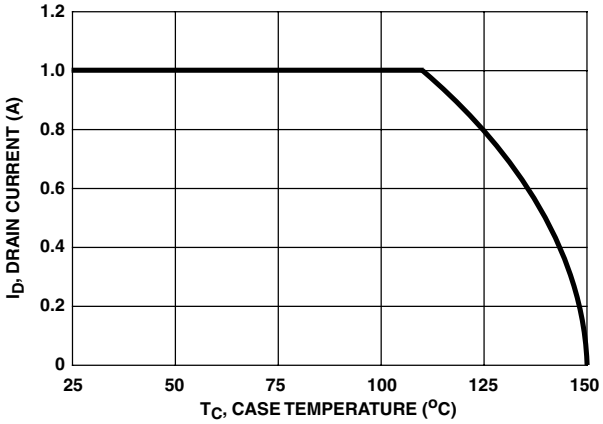


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

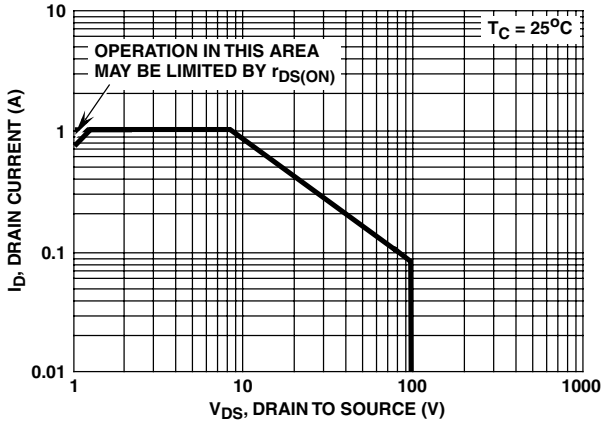


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

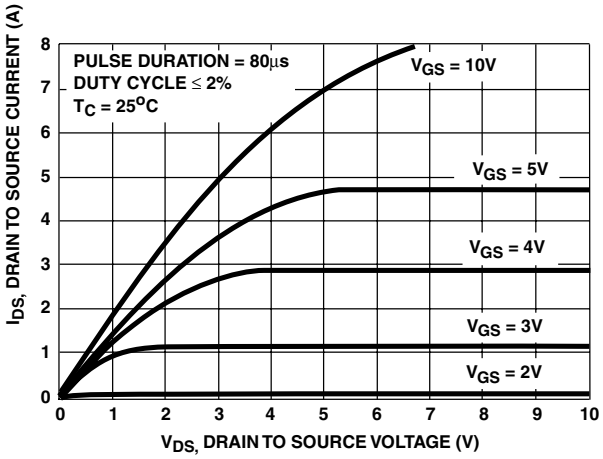


FIGURE 4. SATURATION CHARACTERISTICS

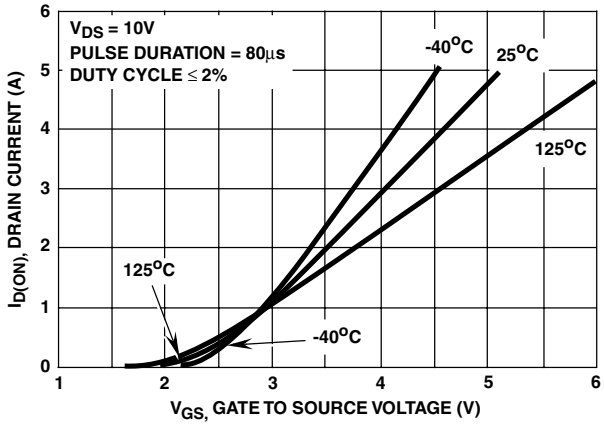


FIGURE 5. TRANSFER CHARACTERISTICS

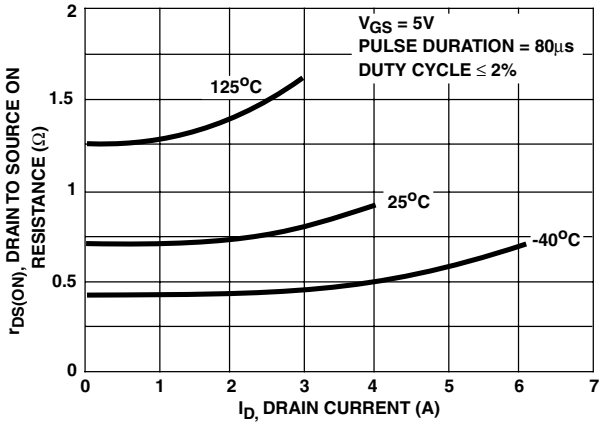


FIGURE 6. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

Typical Performance Curves Unless Otherwise Specified (Continued)

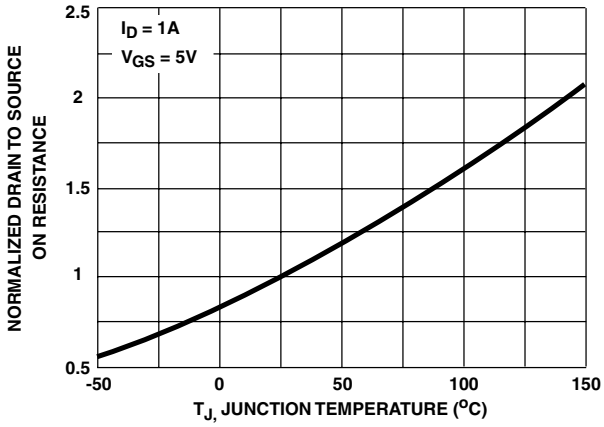


FIGURE 7. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

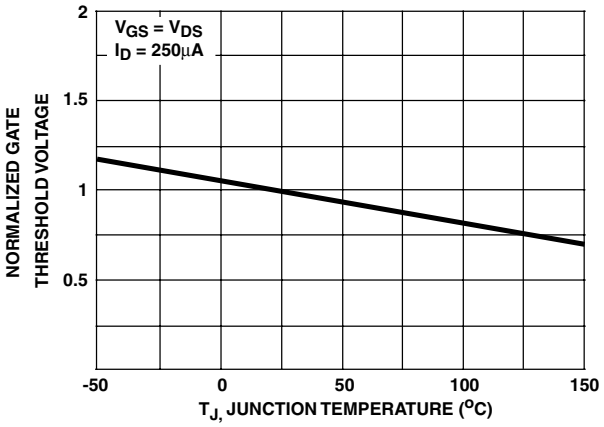


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

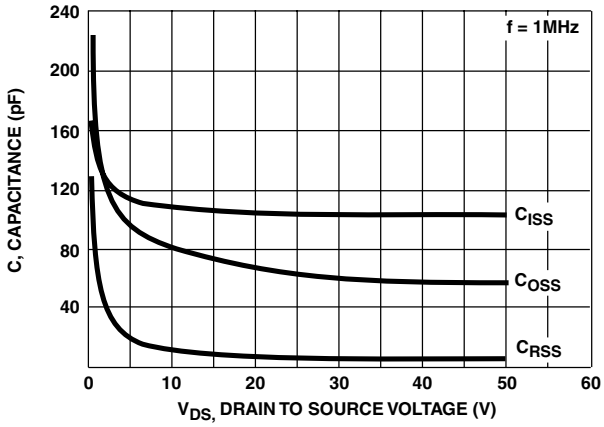
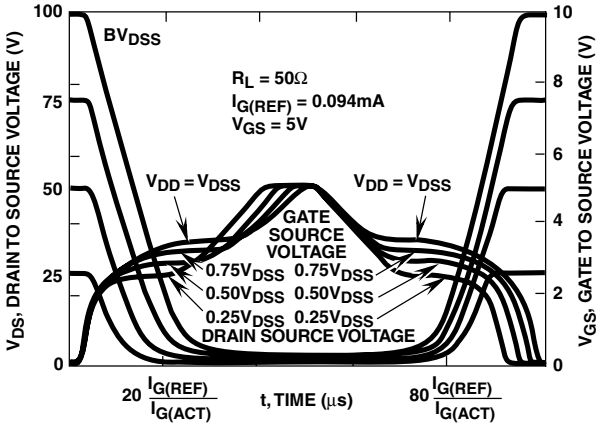


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 10. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

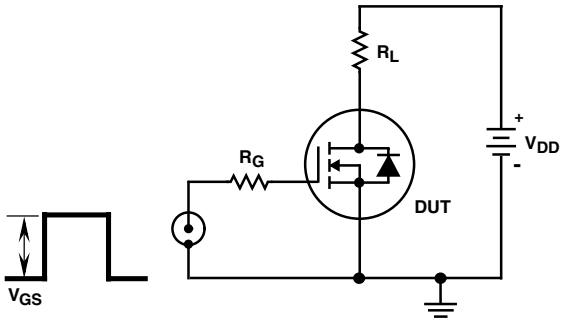


FIGURE 11. SWITCHING TIME TEST CIRCUIT

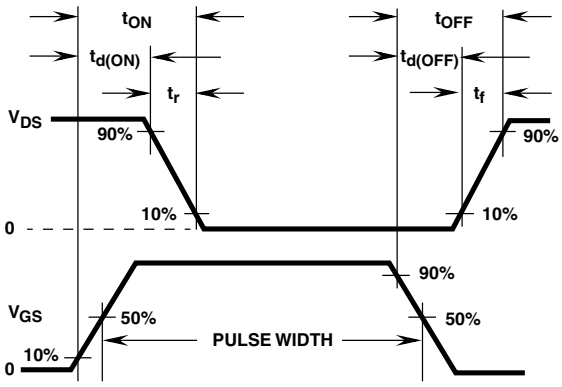


FIGURE 12. RESISTIVE SWITCHING WAVEFORMS

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