

30A, 60V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

March 1995

Features

- 30A, 60V
- $r_{DS(ON)} = 0.065\Omega$
- Temperature Compensating PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG30P06, RFP30P06, RF1S30P06, and RF1S30P06SM P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

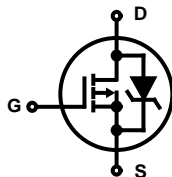
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG30P06	TO-247	RFG30P06
RFP30P06	TO-220AB	RFP30P06
RF1S30P06	TO-262AA	F1S30P06
RF1S30P06SM	TO-263AB	F1S30P06

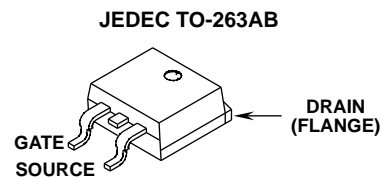
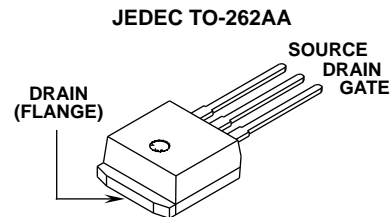
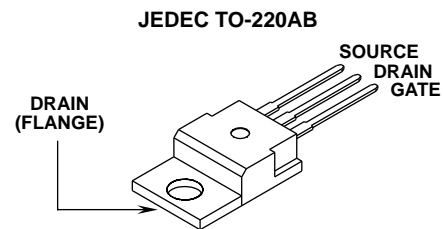
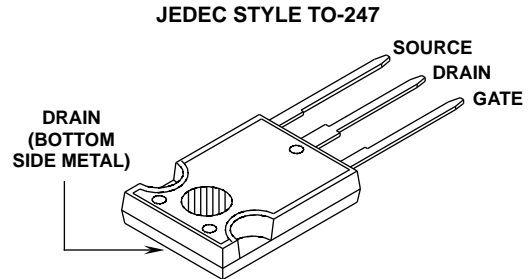
NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S30P06SM9A.

Formerly developmental type TA09834.

Symbol



Packages



Absolute Maximum Ratings $T_C = +25^\circ\text{C}$

	RFG30P06, RFP30P06 RF1S30P06, RF1S30P06SM	UNITS
Drain Source Voltage	-60	V
Drain Gate Voltage	-60	V
Gate Source Voltage	± 20	V
Drain Current		
RMS Continuous	30	A
Pulsed Drain Current	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	Refer to UIS Curve	
Power Dissipation		
$T_C = +25^\circ\text{C}$	120	W
Derate above $+25^\circ\text{C}$	0.9	W/°C
Operating and Storage Temperature	-55 to +175	°C
Soldering Temperature of Leads for 10s	260	°C

Specifications RFG30P06, RFP30P06, RF1S30P06, RF1S30P06SM

Electrical Specifications $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$	-60	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	-2	-	-4	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60\text{V}$, $V_{GS} = 0\text{V}$	$T_C = +25^\circ\text{C}$	-	-	-1	μA
			$T_C = +150^\circ\text{C}$	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	100	nA	
On Resistance	$r_{DS(ON)}$	$I_D = 30\text{A}$, $V_{GS} = -10\text{V}$	-	-	0.065	Ω	
Turn-On Time	t_{ON}	$V_{DD} = -30\text{V}$, $I_D = 15\text{A}$ $R_L = 2.00\Omega$, $V_{GS} = -10\text{V}$ $R_{GS} = 6.25\Omega$	-	-	80	ns	
Turn-On Delay Time	$t_{D(ON)}$		-	15	-	ns	
Rise Time	t_R		-	23	-	ns	
Turn-Off Delay Time	$t_{D(OFF)}$		-	28	-	ns	
Fall Time	t_F		-	18	-	ns	
Turn-Off Time	t_{OFF}		-	-	100	ns	
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 0$ to -20V	$V_{DD} = -48\text{V}$, $I_D = 30\text{A}$, $R_L = 1.6\Omega$	-	140	170
Gate Charge at -10V	$Q_{G(-10)}$	$V_{GS} = 0$ to -10V	-		70	85	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to -2V	-		5.5	6.6	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	3200	-	pF	
Output Capacitance	C_{OSS}		-	800	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	175	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.11	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	80	$^\circ\text{C/W}$	

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -30\text{A}$	-	-	-1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -30\text{A}$, $dI_{SD}/dt = -100\text{A}/\mu\text{s}$	-	-	150	ns

Typical Performance Curves

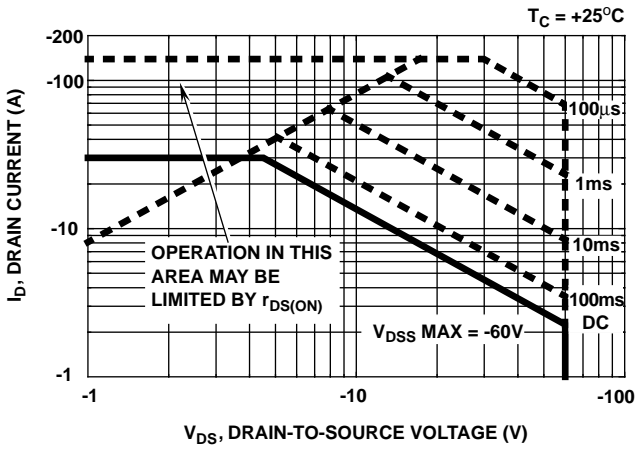


FIGURE 1. SAFE OPERATING AREA CURVE

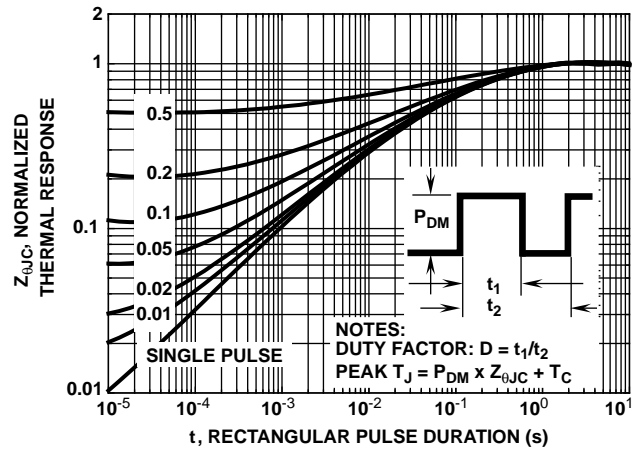


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

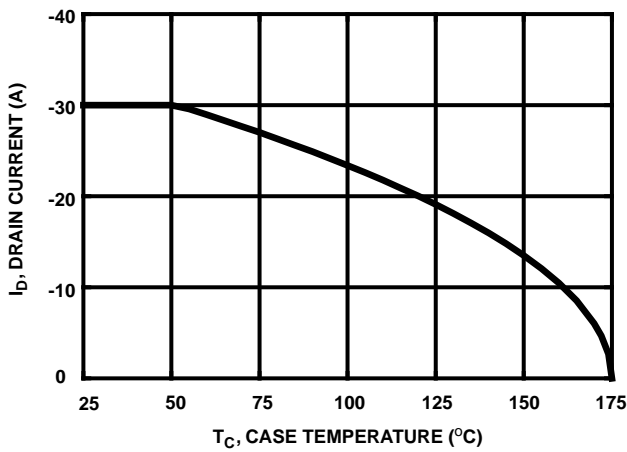


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

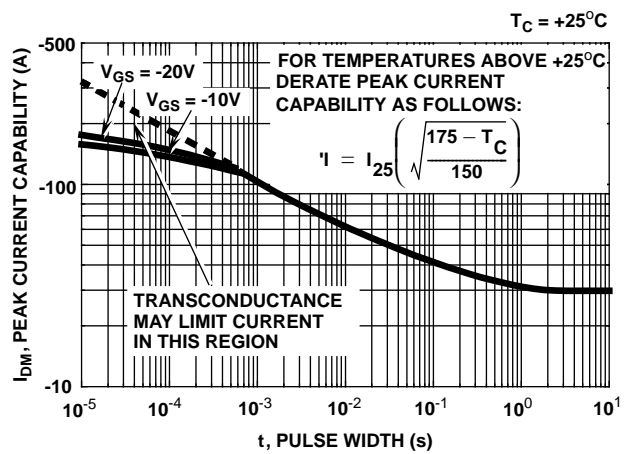


FIGURE 4. PEAK CURRENT CAPABILITY

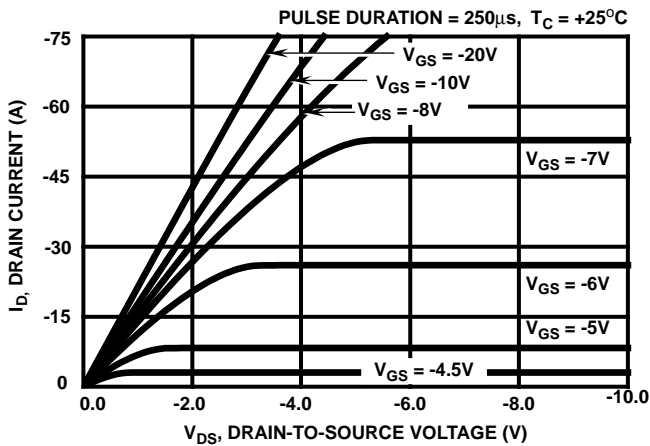


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

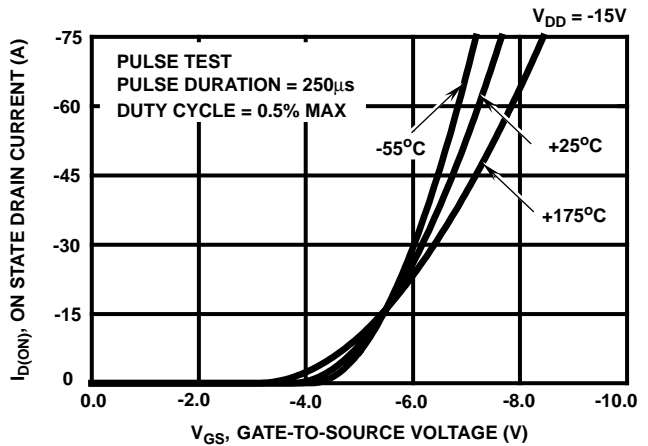


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

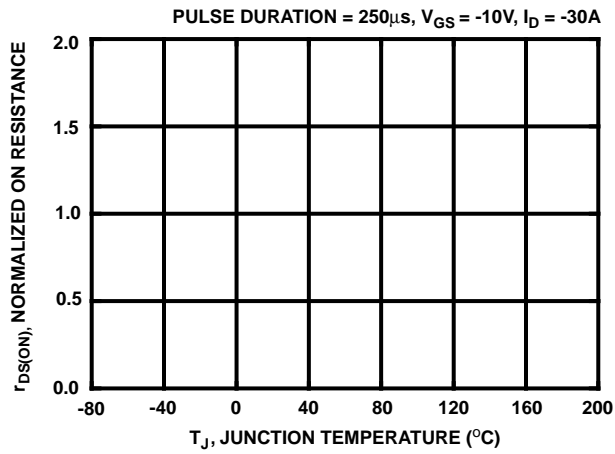


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

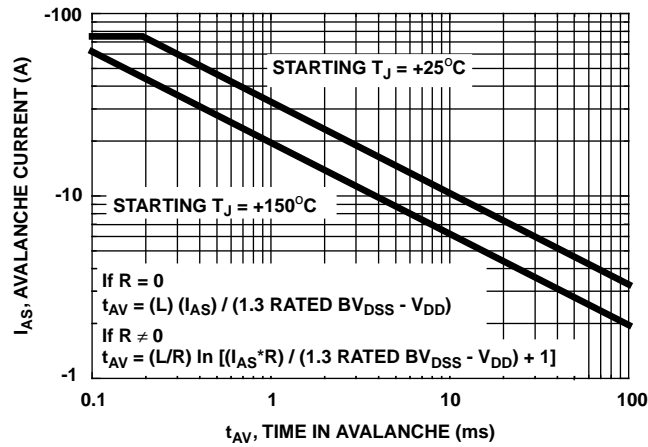


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

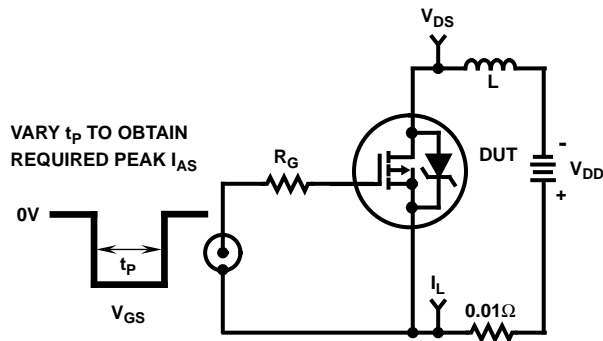


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

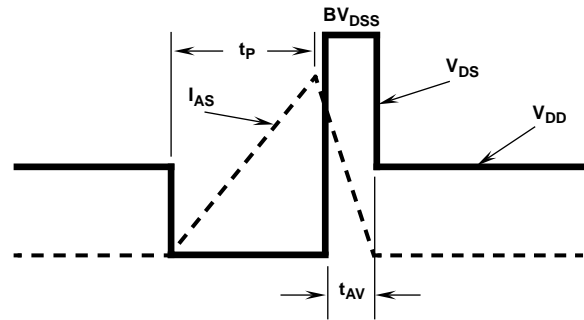


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

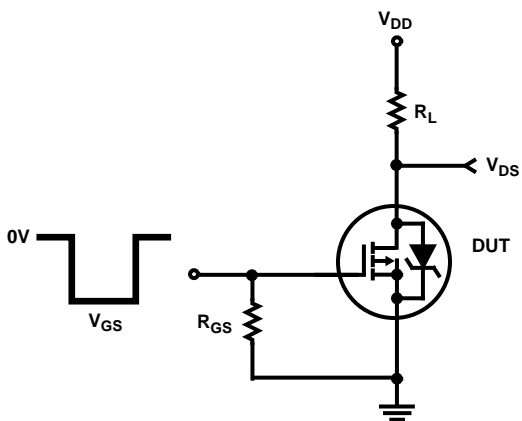


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

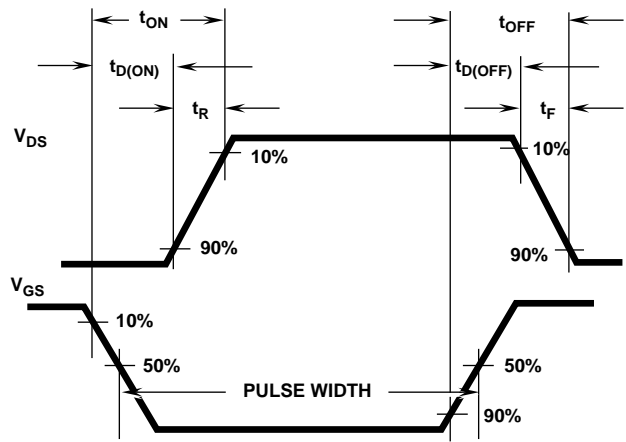


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

RFG30P06, RFP30P06, RF1S30P06, RF1S30P06SM

**Temperature Compensated PSPICE Model for the
RFG30P06, RFP30P06, RF1S30P06, RF1S30P06SM**

.SUBCKT RFP30P06 2 1 3;
REV 8/21/94

CA 12 8 3.23e-9
CB 15 14 3.23e-9
CIN 6 8 3.08e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -77.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.92e-9
LSOURCE 3 7 4.60e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 39.85e-3
RGATE 9 20 2.34
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 2.56e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.81

ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/114,5))}

.MODEL DBDMOD D (IS=4.7e-13 RS=1.31e-2 TRS1=1.39e-4 TRS2=-4.77e-6 CJO=2.85e-9 TT=8.81e-8)
.MODEL DBKMOD D (RS=2.23e-1 TRS1=1.97e-3 TRS2=-2.37e-5)
.MODEL DPLCAPMOD D (CJO=0.78e-9 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.75 KP=10.83 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.08e-4 TC2=-1.72e-6)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=1.02e-5)
.MODEL RSCLMOD RES (TC1=2.09e-3 TC2=5.88e-7)
.MODEL RVTOMOD RES (TC1=-2.99e-3 TC2=1.40e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.4 VOFF=1.4)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.4 VOFF=3.4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.2 VOFF=-3.8)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.8 VOFF=1.2)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.

