

## N-Channel Power MOSFET (97A, 100Volts)

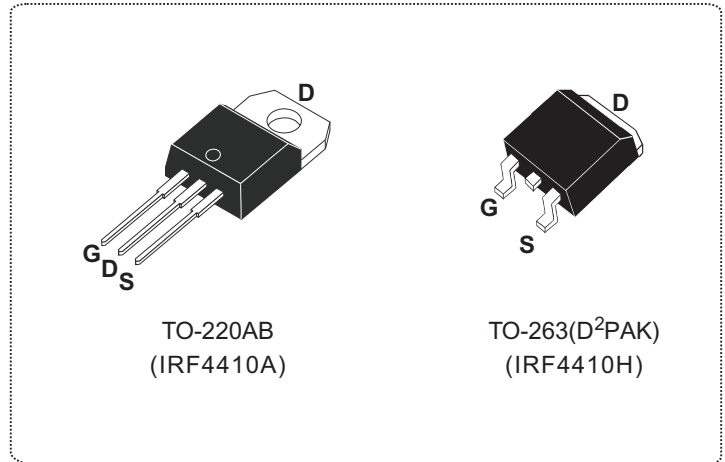
### DESCRIPTION

The Nell **IRF4410** is a three-terminal silicon device with current conduction capability of 97A, fast switching speed, low on-state resistance, breakdown voltage rating of 100V, and max. threshold voltage of 4 volts.

They are designed for use in applications, such as switched mode power supplies, DC to DC converters, **PWM** motor controls, bridge circuits, UPS and general purpose switching applications.

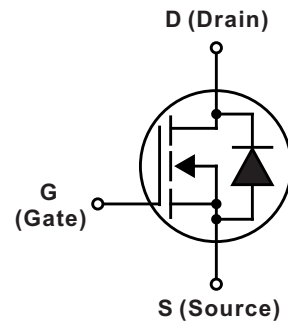
### FEATURES

- $R_{DS(ON)} = 9.0m\Omega @ V_{GS} = 10V$
- Ultra low gate charge(120nC max.)
- Low reverse transfer capacitance ( $C_{RSS} = 170pF$  typical)
- Fast switching capability
- 100% avalanche energy specified
- Improved dv/dt capability
- 175°C operation temperature



TO-220AB  
(IRF4410A)

TO-263(D<sup>2</sup>PAK)  
(IRF4410H)



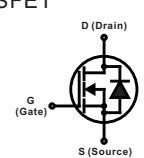
PRODUCT SUMMARY	
$I_D$ (A)	97
$V_{DSS}$ (V)	100
$R_{DS(ON)}$ (m $\Omega$ )	9.0 @ $V_{GS} = 10V$
$Q_G$ (nC) max.	120

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ C$ unless otherwise specified)				
SYMBOL	PARAMETER	TEST CONDITIONS	VALUE	UNIT
$V_{DSS}$	Drain to Source voltage	$T_J = 25^\circ C$ to $150^\circ C$	100	V
$V_{DGR}$	Drain to Gate voltage	$R_{GS} = 20K\Omega$	100	
$V_{GS}$	Gate to Source voltage		$\pm 20$	
$I_D$	Continuous Drain Current	$T_C = 25^\circ C$	97	A
		$T_C = 100^\circ C$	69	
$I_{DM}$	Pulsed Drain current(Note 1)		390	
$I_{AR}$	Avalanche current(Note 1)		58	
$E_{AR}$	Repetitive avalanche energy(Note 1)	$I_{AR} = 58A, R_{GS} = 50\Omega, V_{GS} = 10V$	105	mJ
$E_{AS}$	Single pulse avalanche energy(Note 2)	$I_{AS} = 58A, L = 0.143mH$	242	
dv/dt	Peak diode recovery dv/dt(Note 3)		16	V/ns
$P_D$	Total power dissipation	$T_C = 25^\circ C$	230	W
$T_J$	Operation junction temperature		-55 to 175	°C
$T_{STG}$	Storage temperature		-55 to 175	
$T_L$	Maximum soldering temperature, for 10 seconds	1.6mm from case	300	
	Mounting torque, #6-32 or M3 screw		10 (1.1)	lbf-in (N·m)

Note: 1. Repetitive rating: pulse width limited by junction temperature.  
 2.  $I_{AS} = 58A, V_{DD} = 50V, L = 0.143mH, R_{GS} = 25\Omega$ , starting  $T_J = 25^\circ C$ .  
 3.  $I_{SD} \leq 58A, di/dt \leq 610A/\mu s, V_{DD} \leq V_{(BR)DSS}$ , starting  $T_J \leq 175^\circ C$ .

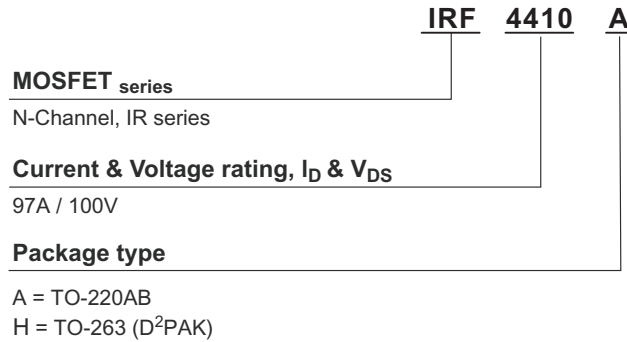
THERMAL RESISTANCE						
SYMBOL	PARAMETER	Min.	Typ.	Max.	UNIT	
$R_{th(j-c)}$	Thermal resistance, junction to case			0.65	°C/W	
$R_{th(j-a)}$	Thermal resistance, junction to ambient	TO-220AB		62		
		TO-263(D <sup>2</sup> PAK)		40		

ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{(BR)DSS}$	Drain to source breakdown voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100			V
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown voltage temperature coefficient	$I_D = 5\text{mA}, V_{DS} = V_{GS}$		0.12		V/°C
$I_{DSS}$	Drain to source leakage current	$V_{DS} = 100\text{V}, V_{GS} = 0\text{V}$ $T_C = 25^\circ\text{C}$			10	μA
		$V_{DS} = 80\text{V}, V_{GS} = 0\text{V}$ $T_C = 125^\circ\text{C}$			100	
$I_{GSS}$	Gate to source forward leakage current	$V_{GS} = 20\text{V}, V_{DS} = 0\text{V}$			100	nA
	Gate to source reverse leakage current	$V_{GS} = -20\text{V}, V_{DS} = 0\text{V}$			-100	
$R_{DS(ON)}$	Static drain to source on-state resistance	$I_D = 58\text{A}, V_{GS} = 10\text{V}$		7.2	9.0	mΩ
$V_{GS(TH)}$	Gate threshold voltage	$V_{GS} = V_{DS}, I_D = 150\mu\text{A}$	2.0		4.0	V
$R_G$	Internal gate resistance			0.7		Ω
$g_{fs}$	Forward transconductance	$I_D = 58\text{A}, V_{DS} = 10\text{V}$	140			S
$C_{ISS}$	Input capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		4820		pF
$C_{OSS}$	Output capacitance			340		
$C_{RSS}$	Reverse transfer capacitance			170		
$t_{d(ON)}$	Turn-on delay time	$V_{DD} = 65\text{V}, V_{GS} = 10\text{V}, I_D = 58\text{A}, R_{GS} = 2.7\Omega$ (Note 1, 2)		16		ns
$t_r$	Rise time			52		
$t_{d(OFF)}$	Turn-off delay time			43		
$t_f$	Fall time			57		
$Q_G$	Total gate charge	$V_{DD} = 50\text{V}, V_{GS} = 10\text{V}, I_D = 58\text{A}$ (Note 1, 2)		83	120	nC
$Q_{GS}$	Gate to source charge			19		
$Q_{GD}$	Gate to drain charge (Miller charge)			27		

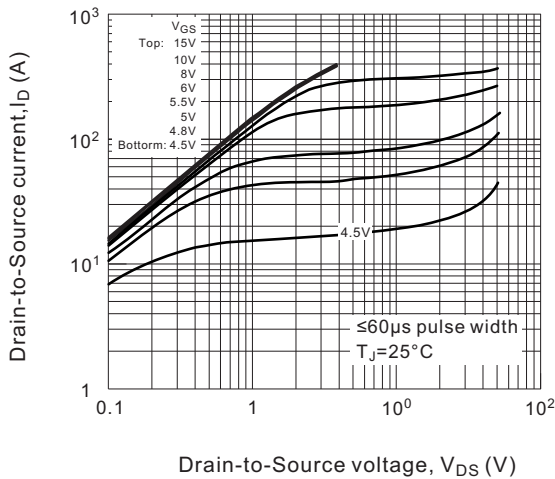
SOURCE TO DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise specified)						
SYMBOL	PARAMETER	TEST CONDITIONS	Min.	Typ.	Max.	UNIT
$V_{SD}$	Diode forward voltage	$I_{SD} = 58\text{A}, V_{GS} = 0\text{V}$			1.3	V
$I_S (I_{SD})$	Continuous source to drain current	Integral reverse P-N junction diode in the MOSFET 			97	A
$I_{SM}$	Pulsed source current				390	
$t_{rr}$	Reverse recovery time	$I_{SD} = 58\text{A}, V_R = 85\text{V}, di_F/dt = 100\text{A}/\mu\text{s}$		38	60	ns
$Q_{rr}$	Reverse recovery charge			53	80	nC
$t_{ON}$	Forward turn-on time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Note: 1. Pulse test: Pulse width  $\leq 400\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 2. Essentially independent of operating temperature.

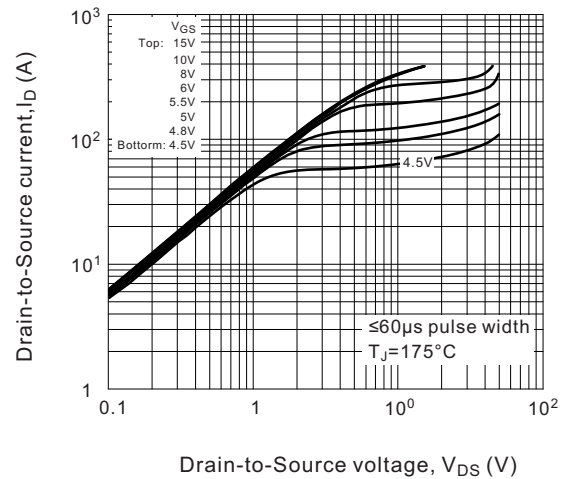
## ORDERING INFORMATION SCHEME



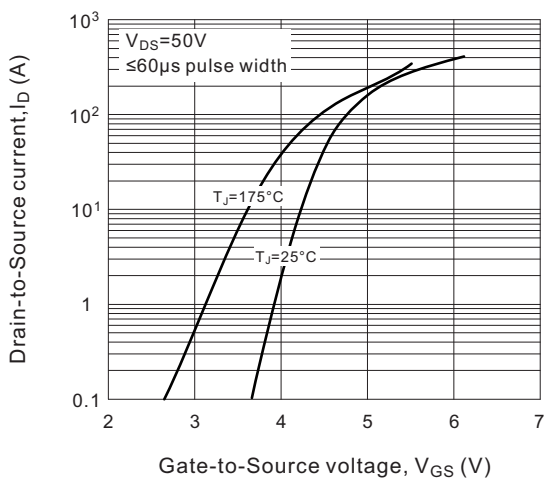
**Fig.1 Typical output characteristics**



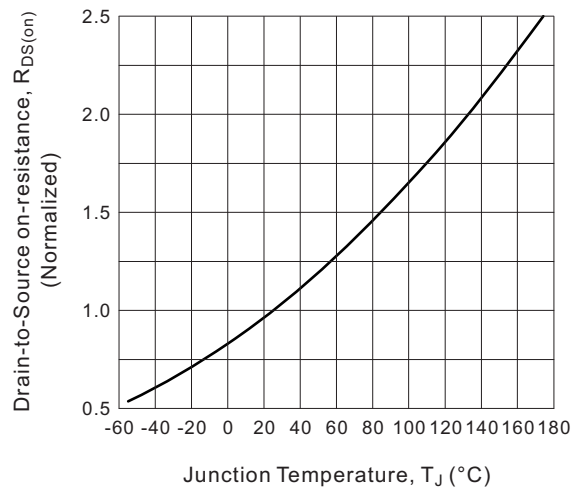
**Fig.2 Typical output characteristics**



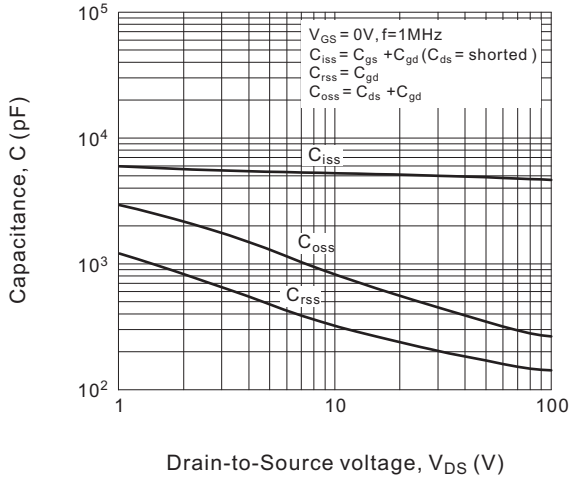
**Fig.3 Typical transfer characteristics**



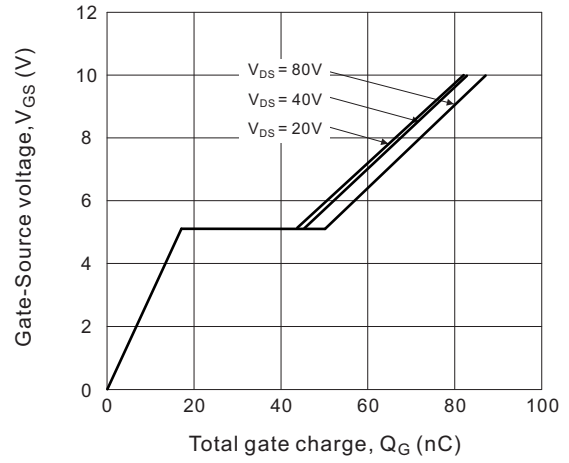
**Fig.4 Normalized on-resistance vs. Junction temperature**



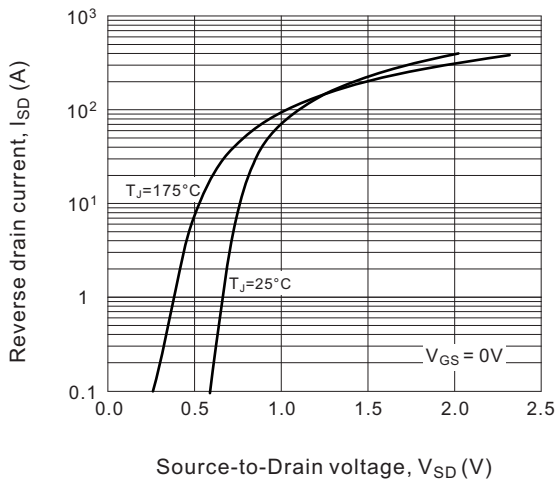
**Fig.5 Typical capacitance vs. Drain-to-Source voltage**



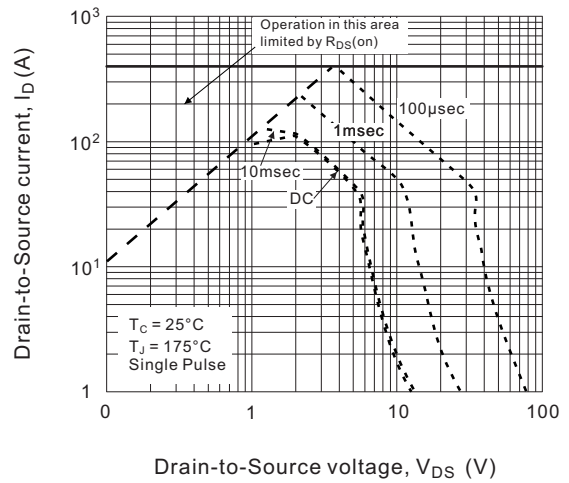
**Fig.6 Typical gate charge vs. Gate-to-Source voltage**



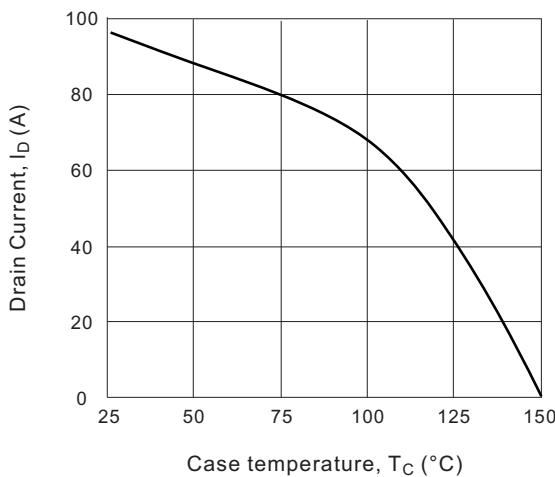
**Fig.7 Typical Source-Drain diode forward voltage**



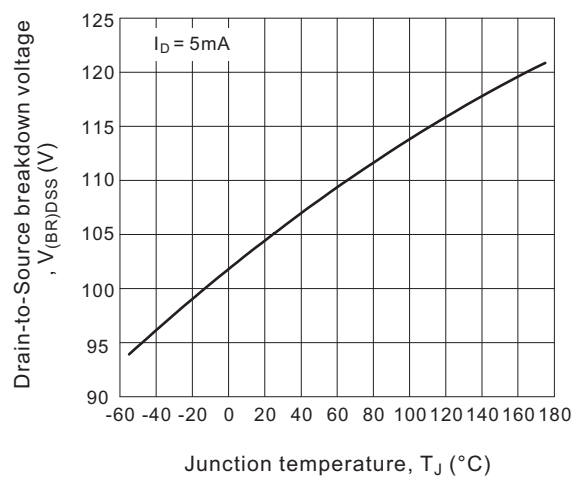
**Fig.8 Maximum safe operating area**



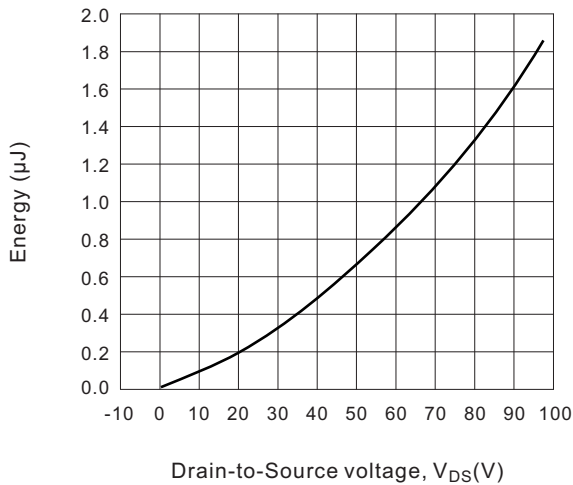
**Fig.9 Maximum drain current vs. Case temperature**



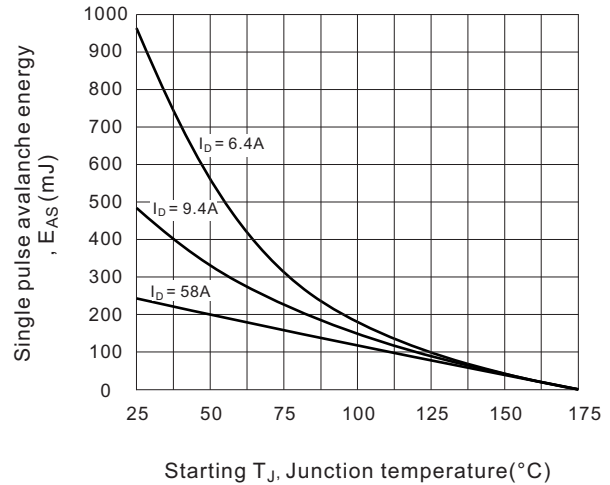
**Fig.10 Drain-to-Source breakdown voltage vs. Junction temperature**



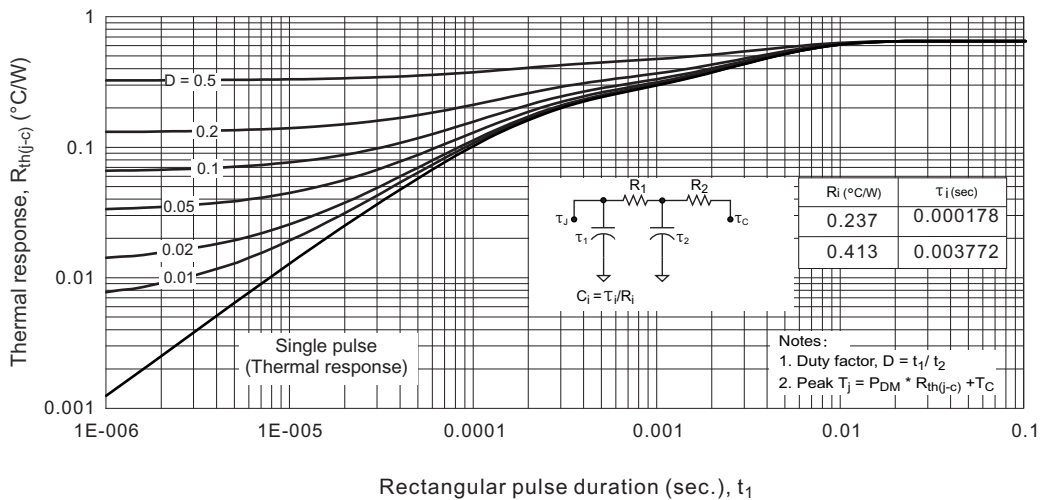
**Fig.11 Typical C<sub>oss</sub> stored energy**



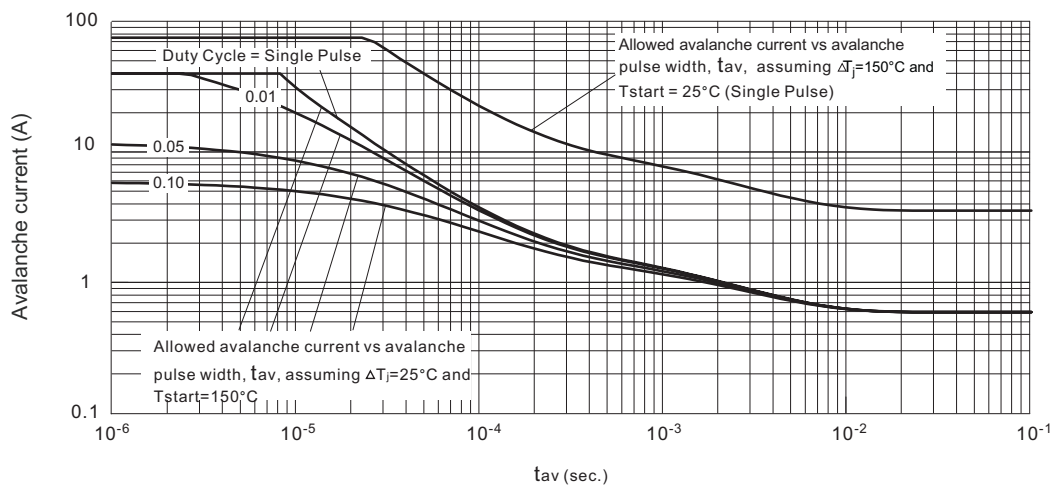
**Fig.12 Maximum avalanche energy vs. Drain current**



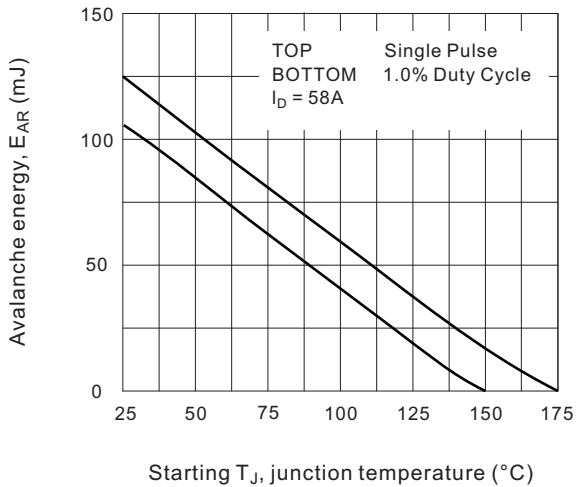
**Fig.13 Maximum effective transient thermal Impedance, Junction-to-Case**



**Fig.14 Typical avalanche current vs. Pulse width**



**Fig.15 Maximum avalanche energy vs. Junction temperature**



**Notes on Repetitive Avalanche Curves. Fig. 14, 15:**

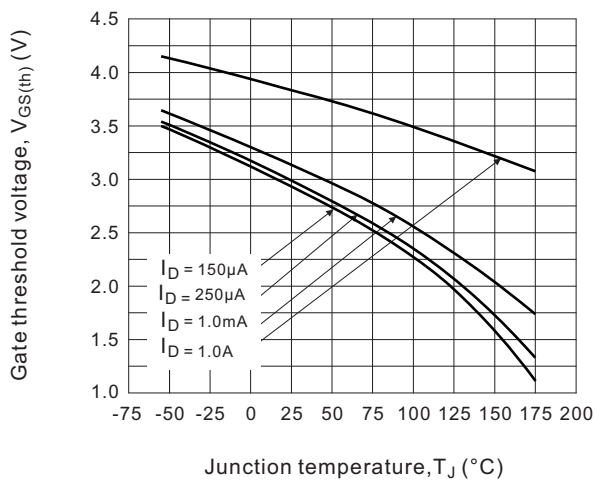
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{max}$  (assumed as 25°C in Fig.14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $R_{th(j-c)}$  ( $D, t_{av}$ ) = Transient thermal resistance, see fig.13

$$P_{D(ave)} = \frac{1}{2} (1.3 \cdot BV \cdot I_{av}) = \Delta T / R_{th(j-c)}$$

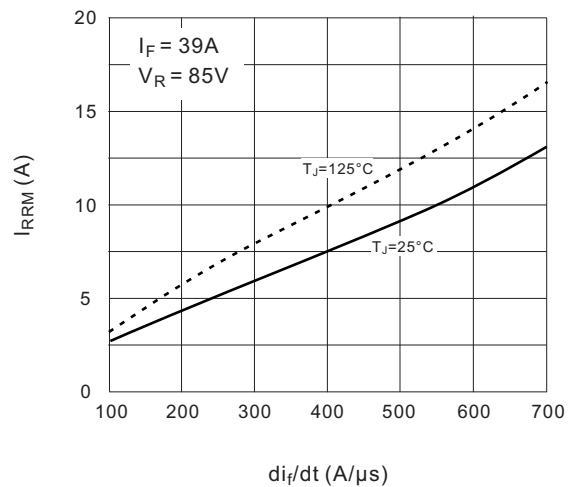
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot R_{th(j-c)}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

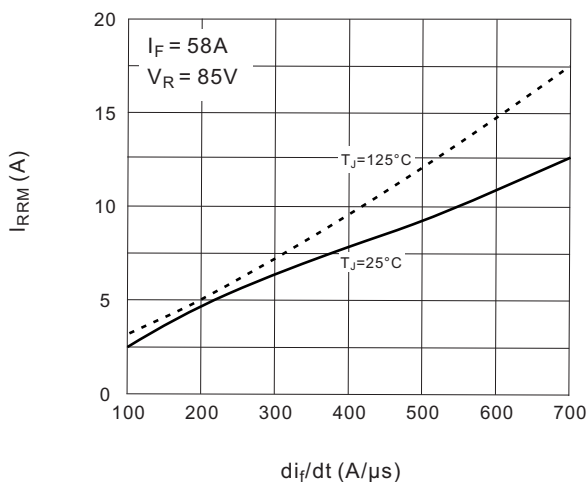
**Fig.16 Threshold voltage vs. Junction Temperature**



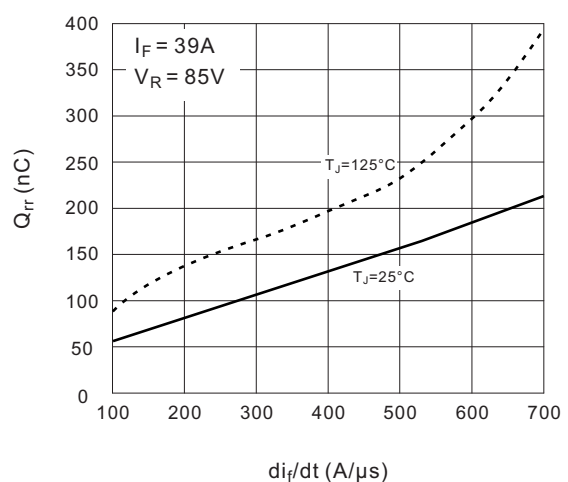
**Fig.17 Typical recovery current vs. di\_t/dt**



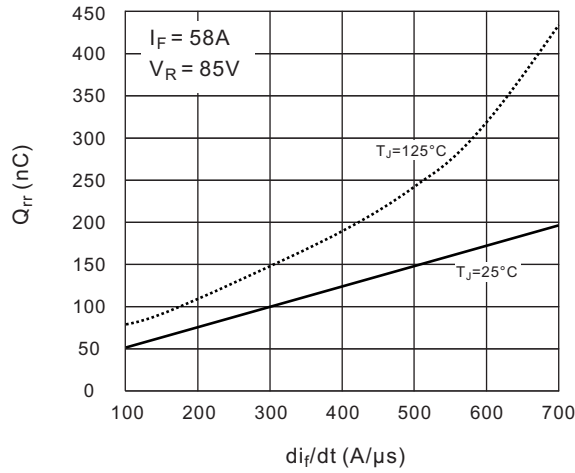
**Fig.18 Typical recovery current vs. di\_t/dt**



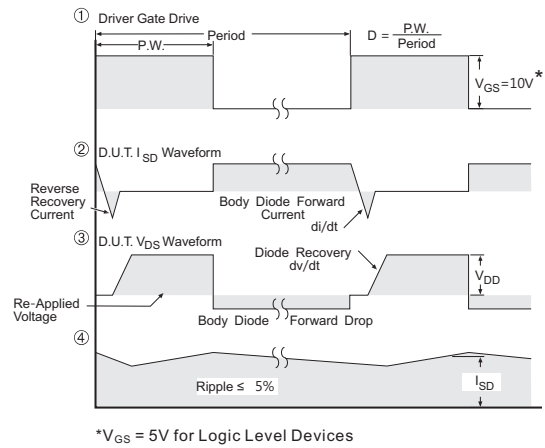
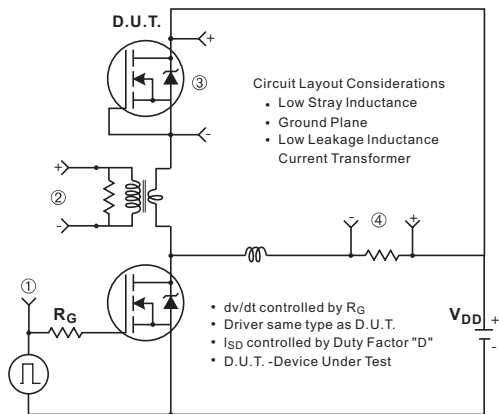
**Fig.19 Typical stored charge vs. di\_t/dt**



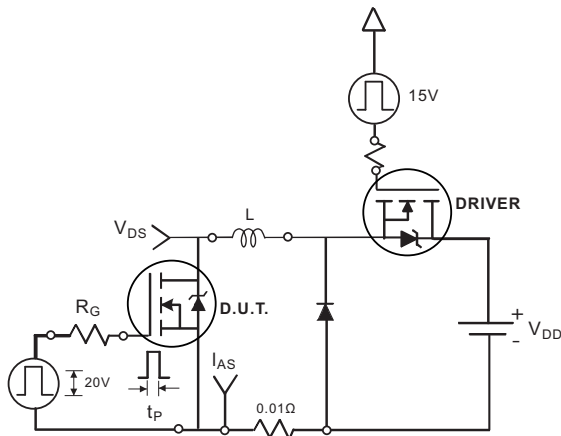
**Fig.20 Typical stored charge vs. di/dt**



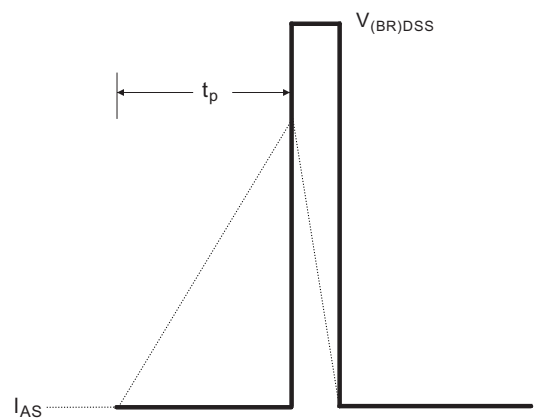
**Fig.21 Peak diode recovery dv/dt test circuit for N-Channel**



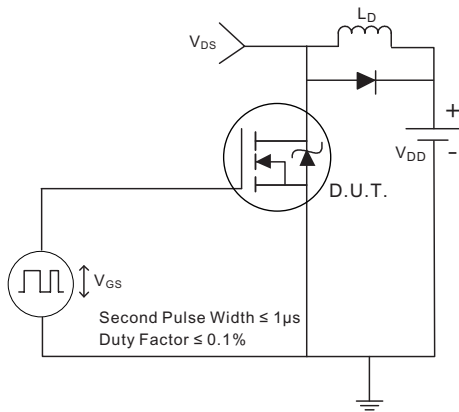
**Fig.22a Unclamped Inductive test circuit**



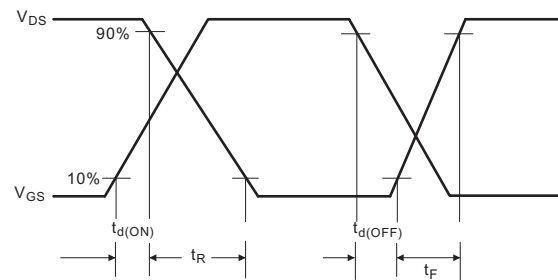
**Fig.22b Unclamped inductive waveforms**



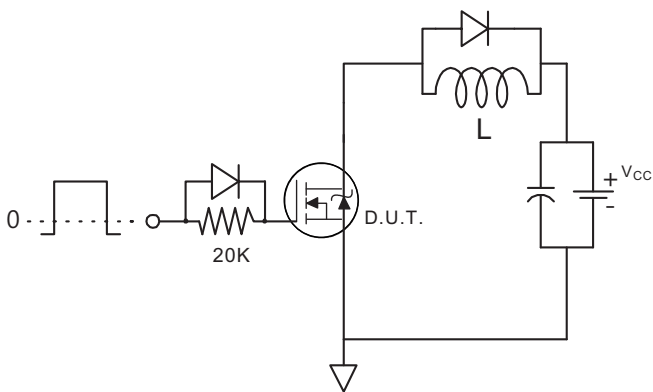
**Fig.23a Switching time test circuit**



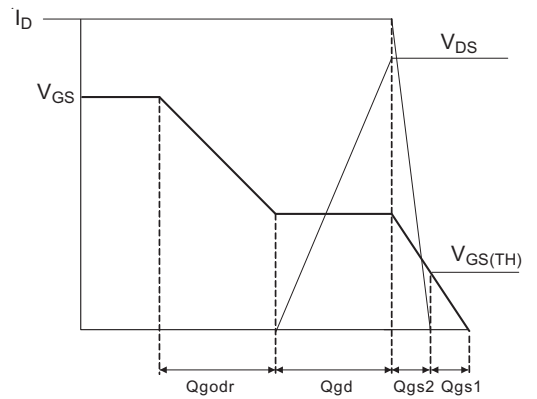
**Fig.23b Switching time Waveforms**



**Fig.24a Gate charge test circuit**



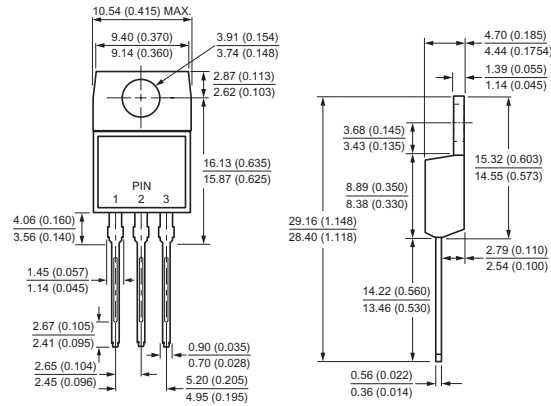
**Fig.24b Gate charge waveform**



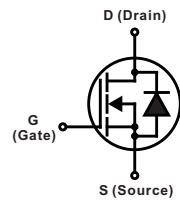
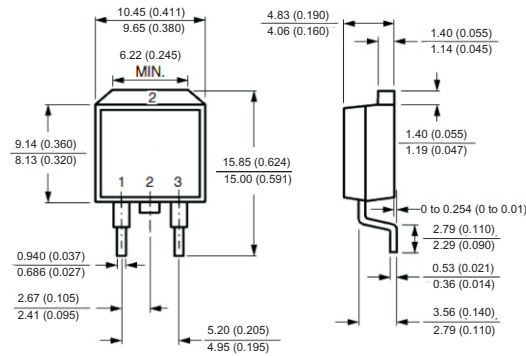


## Case Style

### TO-220AB



### TO-263(D<sup>2</sup>PAK)



All dimensions in millimeters(inches)