

NTF6P02T3G, NVF6P02T3G

Power MOSFET -10 Amps, -20 Volts

P-Channel SOT-223

Features

- Low $R_{DS(on)}$
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- AEC Q101 Qualified and PPAP Capable – NVF6P02T3G
- NVF Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Power Management in Portables and Battery-Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	-20	Vdc
Gate-to-Source Voltage	V_{GS}	± 8.0	Vdc
Drain Current (Note 1)			
– Continuous @ $T_A = 25^\circ\text{C}$	I_D	-10	Adc
– Continuous @ $T_A = 70^\circ\text{C}$	I_D	-8.4	
– Single Pulse ($t_p = 10 \mu\text{s}$)	I_{DM}	-35	Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	8.3	W
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = -20 \text{ Vdc}$, $V_{GS} = -5.0 \text{ Vdc}$, $I_{L(pk)} = -10 \text{ A}$, $L = 3.0 \text{ mH}$, $R_G = 25\Omega$)	E_{AS}	150	mJ
Thermal Resistance			$^\circ\text{C}/\text{W}$
– Junction to Lead (Note 1)	$R_{\theta JL}$	15	
– Junction to Ambient (Note 2)	$R_{\theta JA}$	71.4	
– Junction to Ambient (Note 3)	$R_{\theta JA}$	160	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Steady State.
2. When surface mounted to an FR4 board using 1" pad size, (Cu. Area 1.127 sq in), Steady State.
3. When surface mounted to an FR4 board using minimum recommended pad size, (Cu. Area 0.412 sq in), Steady State.

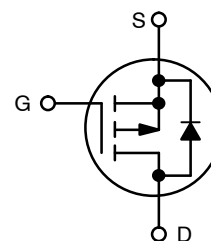


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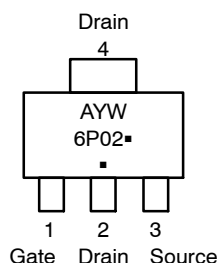
**-10 AMPERES
-20 VOLTS**

$R_{DS(on)} = 44 \text{ m}\Omega$ (Typ.)



P-Channel MOSFET

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
Y = Year
W = Work Week
6P02 = Specific Device Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTF6P02T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NVF6P02T3G	SOT-223 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 4) (V _{GS} = 0 Vdc, I _D = -250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	-20	-25	-	Vdc
		-	-11	-	mV/°C
Zero Gate Voltage Drain Current (V _{DS} = -20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = -20 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	-	-	-1.0	μAdc
		-	-	-10	
Gate-Body Leakage Current (V _{GS} = ± 8.0 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	± 100	nAdc

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage (Note 4) (V _{DS} = V _{GS} , I _D = -250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	-0.4	-0.7	-1.0	Vdc
		-	2.6	-	mV/°C
Static Drain-to-Source On-Resistance (Note 4) (V _{GS} = -4.5 Vdc, I _D = -6.0 Adc) (V _{GS} = -2.5 Vdc, I _D = -4.0 Adc) (V _{GS} = -2.5 Vdc, I _D = -3.0 Adc)	R _{DS(on)}	-	44	50	mΩ
		-	57	70	
		-	57	-	
Forward Transconductance (Note 4) (V _{DS} = -10 Vdc, I _D = -6.0 Adc)	g _{fs}	-	12	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = -16 Vdc, V _{GS} = 0 V, f = 1.0 MHz)	C _{iSS}	-	900	1200	pF
Output Capacitance		C _{oSS}	-	350	500	
Transfer Capacitance		C _{rSS}	-	90	150	
Input Capacitance	(V _{DS} = -10 Vdc, V _{GS} = 0 V, f = 1.0 MHz)	C _{iSS}	-	940	-	pF
Output Capacitance		C _{oSS}	-	410	-	
Transfer Capacitance		C _{rSS}	-	110	-	

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V _{DD} = -5.0 Vdc, I _D = -1.0 Adc, V _{GS} = -4.5 Vdc, R _G = 6.0 Ω)	t _{d(on)}	-	7.0	12	ns
Rise Time		t _r	-	25	45	
Turn-Off Delay Time		t _{d(off)}	-	75	125	
Fall Time		t _f	-	50	85	
Turn-On Delay Time	(V _{DD} = -16 Vdc, I _D = -6.0 Adc, V _{GS} = -4.5 Vdc, R _G = 2.5 Ω)	t _{d(on)}	-	8.0	-	ns
Rise Time		t _r	-	30	-	
Turn-Off Delay Time		t _{d(off)}	-	60	-	
Fall Time		t _f	-	60	-	
Gate Charge	(V _{DS} = -16 Vdc, I _D = -6.0 Adc, V _{GS} = -4.5 Vdc) (Note 4)	Q _T	-	15	20	nC
		Q _{GS}	-	1.7	-	
		Q _{gd}	-	6.0	-	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = -3.0 Adc, V _{GS} = 0 Vdc) (Note 4) (I _S = -2.1 Adc, V _{GS} = 0 Vdc) (I _S = -3.0 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	-	-0.82	-1.2	Vdc
			-	-0.74	-	
			-	-0.68	-	
Reverse Recovery Time	(I _S = -3.0 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs) (Note 4)	t _{rr}	-	42	-	ns
		t _a	-	17	-	
		t _b	-	25	-	
Reverse Recovery Stored Charge		Q _{RR}	-	0.036	-	μC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL ELECTRICAL CHARACTERISTICS

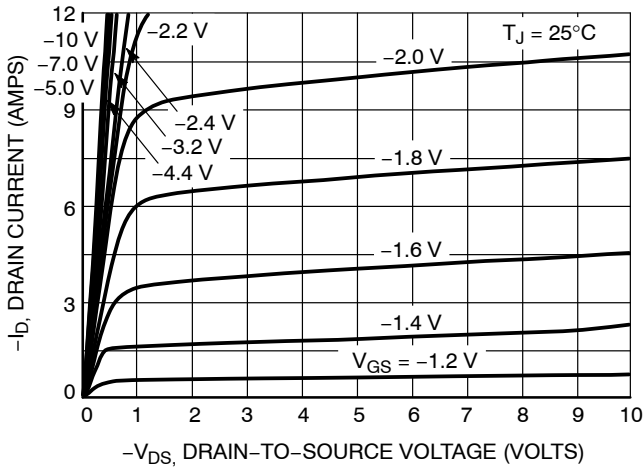


Figure 1. On-Region Characteristics

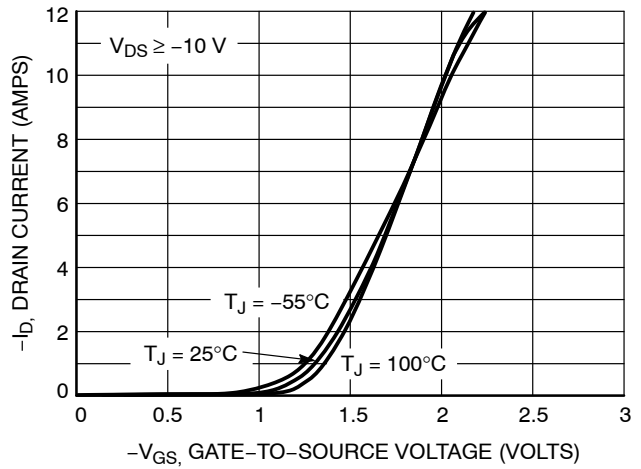


Figure 2. Transfer Characteristics

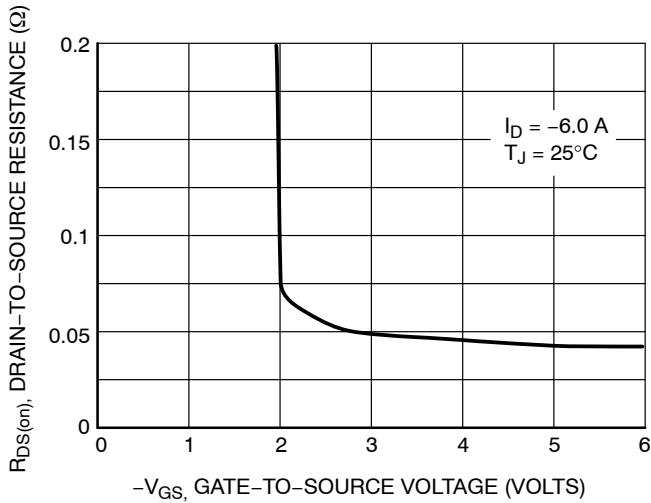


Figure 3. On-Resistance versus Gate-to-Source Voltage

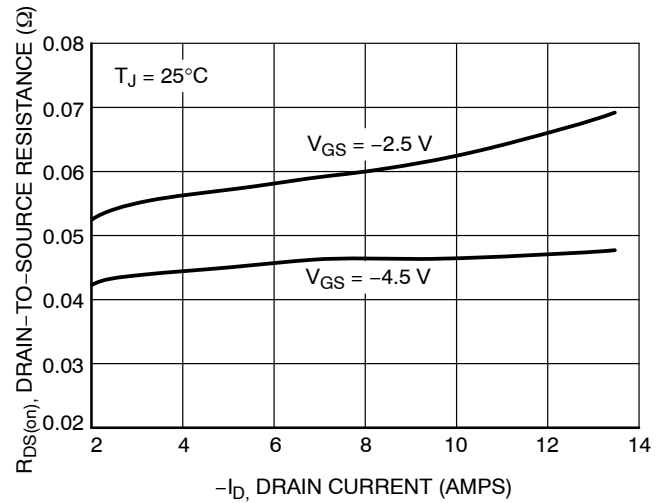


Figure 4. On-Resistance versus Drain Current and Gate Voltage

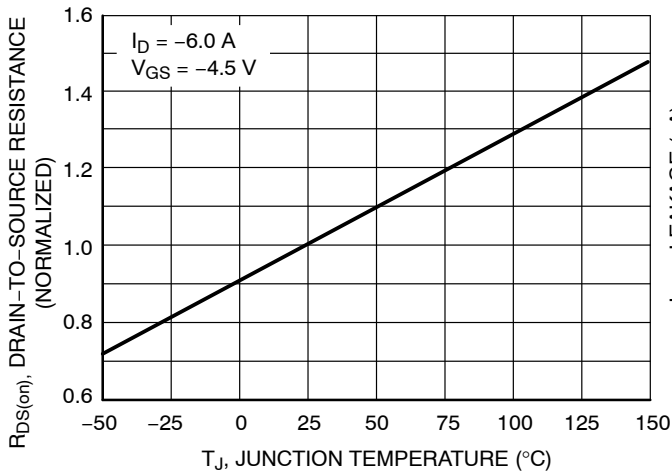


Figure 5. On-Resistance Variation with Temperature

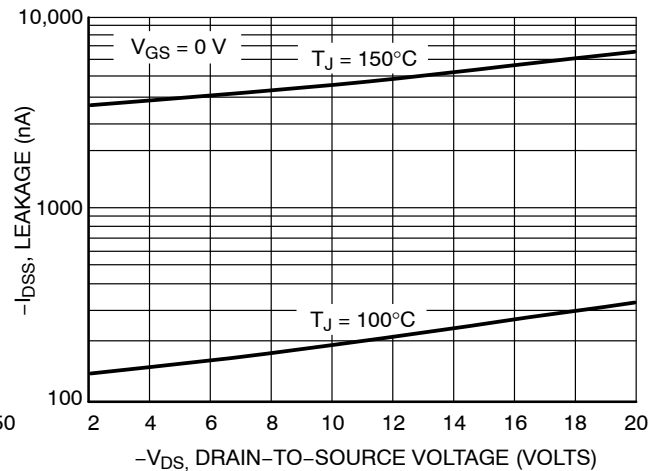


Figure 6. Drain-to-Source Leakage Current versus Voltage

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TYPICAL ELECTRICAL CHARACTERISTICS

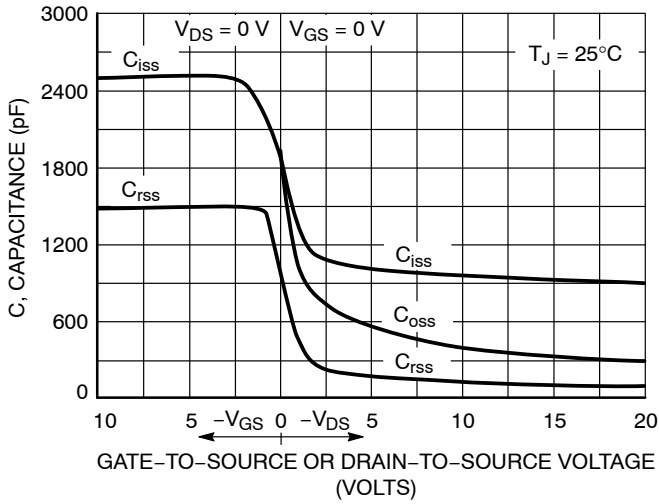


Figure 7. Capacitance Variation

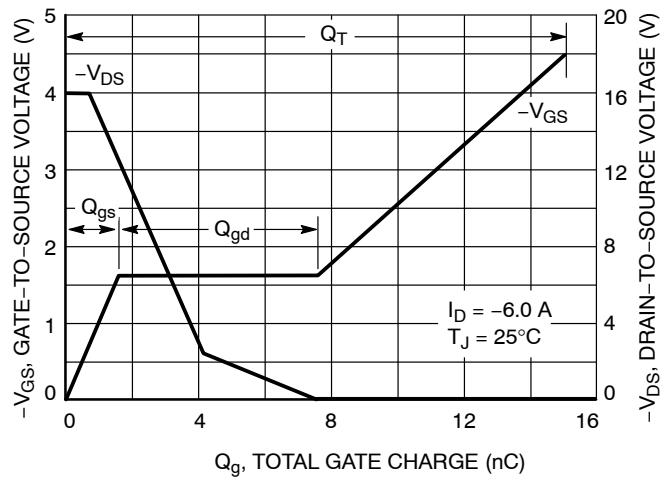


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

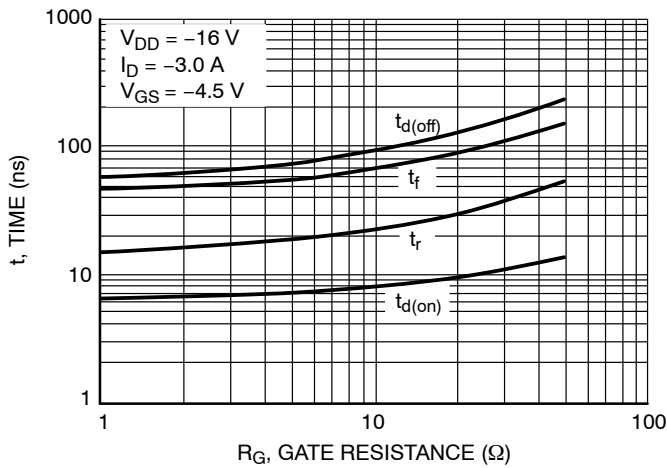


Figure 9. Resistive Switching Time Variation versus Gate Resistance

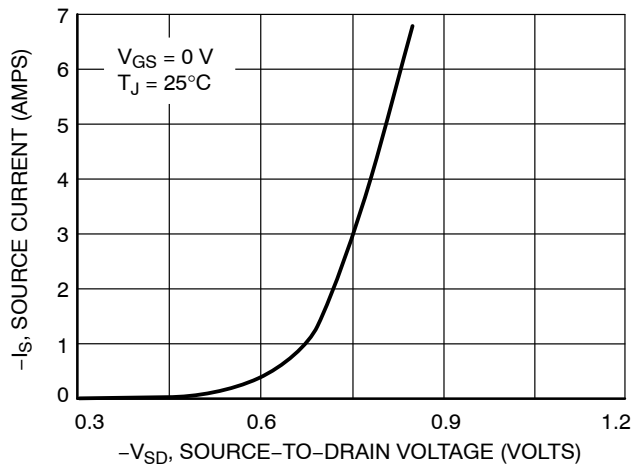


Figure 10. Diode Forward Voltage versus Current

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TYPICAL ELECTRICAL CHARACTERISTICS

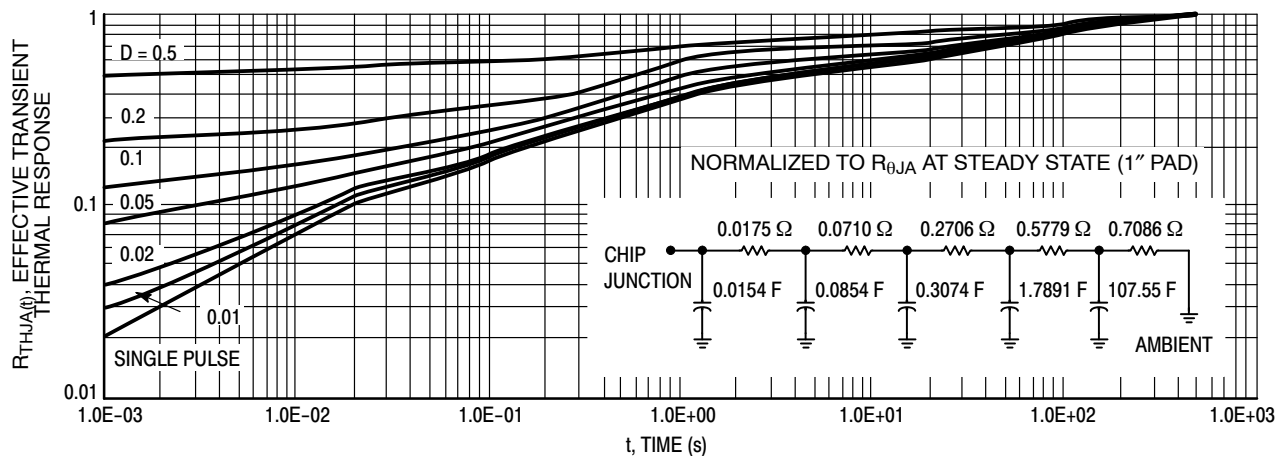
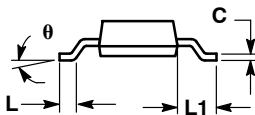
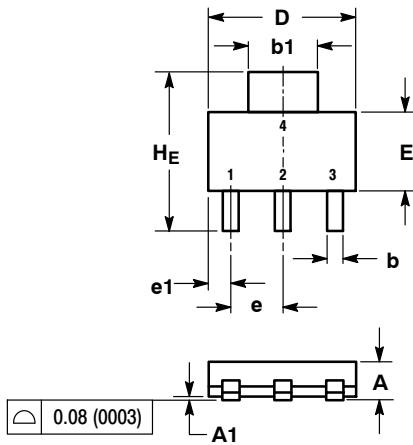


Figure 11. FET Thermal Response

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PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE N



NOTES:

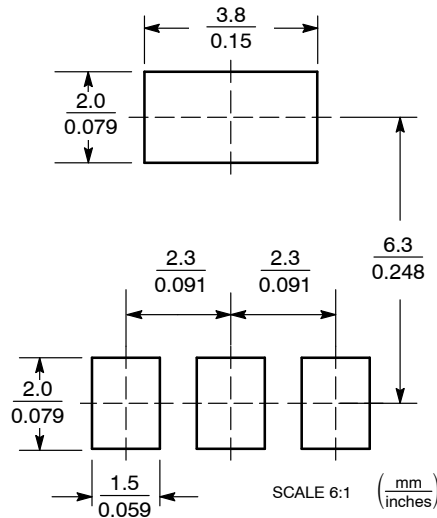
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
theta	0°	---	10°	0°	---	10°

STYLE 3:

1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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