

# NTB5860NL

## Advance Information

### N-Channel Power MOSFET 60 V, 169 A, 3.0 mΩ

#### Features

- Low  $R_{DS(on)}$
- High Current Capability
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	$V_{DSS}$	60	V		
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	V		
Continuous Drain Current, $R_{\theta JA}$	Steady State	$T_A = 25^\circ\text{C}$	169	A	
		$T_A = 100^\circ\text{C}$			119
Power Dissipation, $R_{\theta JA}$	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	167	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	520	A	
Current Limited by Package	$I_{DMmax}$	130	A		
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$		
Source Current (Body Diode)	$I_S$	130	A		
Single Pulse Drain-to-Source Avalanche Energy ( $L = 0.3 \text{ mH}$ )	$E_{AS}$	735	mJ		
Lead Temperature for Soldering Purposes (1/8" from Case for 10 Seconds)	$T_L$	260	$^\circ\text{C}$		

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State	$R_{\theta JC}$	0.9	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	34	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

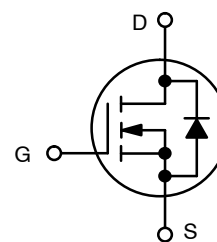
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



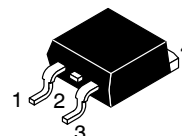
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
60 V	3.0 mΩ @ 10 V	169 A
	3.6 mΩ @ 4.5 V	

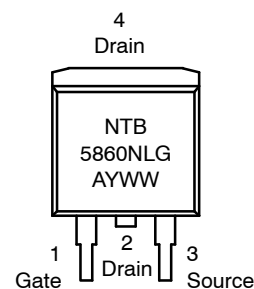


N-CHANNEL MOSFET



D<sup>2</sup>PAK  
CASE 418B  
STYLE 2

#### MARKING DIAGRAM & PIN ASSIGNMENTS



A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Device

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

# NTB5860NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>DS</sub> = 0 V, I <sub>D</sub> = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>	I <sub>D</sub> = 250 μA, ref to 25°C		6.1		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub> = 60 V	T <sub>J</sub> = 25°C		1.0	μA
		V <sub>GS</sub> = 0 V V <sub>DS</sub> = 60 V	T <sub>J</sub> = 125°C		100	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0		3.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(th)</sub> /T <sub>J</sub>			7.7		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		2.4	3.0	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		2.8	3.6	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 30 A		47		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz		13216		pF
Output Capacitance	C <sub>oss</sub>			1127		
Transfer Capacitance	C <sub>rss</sub>			752		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 40 A		115		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 48 V, I <sub>D</sub> = 40 A		220		
Threshold Gate Charge	Q <sub>G(TH)</sub>			13		
Gate-to-Source Charge	Q <sub>GS</sub>			37		
Gate-to-Drain Charge	Q <sub>GD</sub>			54		

### SWITCHING CHARACTERISTICS, V<sub>GS</sub> = 10 V (Note 3)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 48 V, I <sub>D</sub> = 40 A, R <sub>G</sub> = 2.5 Ω		25		ns
Rise Time	t <sub>r</sub>			58		
Turn-Off Delay Time	t <sub>d(off)</sub>			98		
Fall Time	t <sub>f</sub>			144		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V I <sub>S</sub> = 20 A	T <sub>J</sub> = 25°C		0.76	1.1	V <sub>dc</sub>
			T <sub>J</sub> = 125°C		0.60		
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V <sub>dc</sub> , I <sub>S</sub> = 40 A <sub>dc</sub> , dI <sub>S</sub> /dt = 100 A/μs		50		ns	
Charge Time	t <sub>a</sub>			25			
Discharge Time	t <sub>b</sub>			25			
Reverse Recovery Stored Charge	Q <sub>RR</sub>			71			nC

- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- Switching characteristics are independent of operating junction temperatures.

### ORDERING INFORMATION

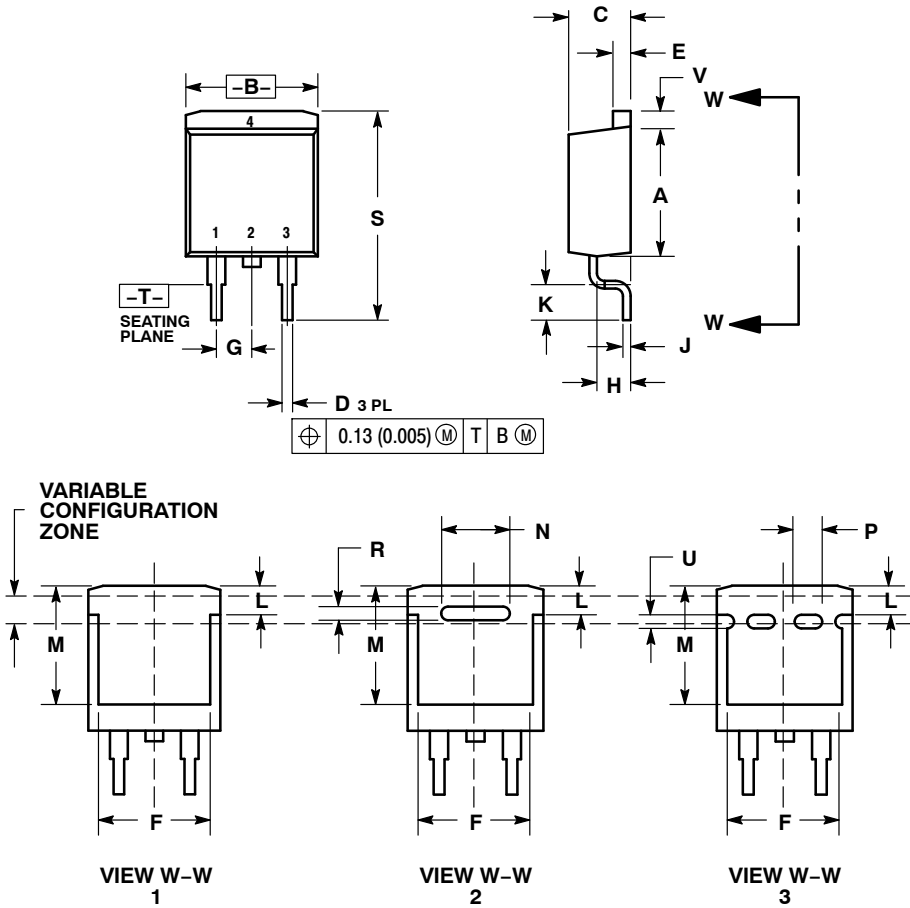
Device	Package	Shipping†
NTB5860NLT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## PACKAGE DIMENSIONS

D<sup>2</sup>PAK  
CASE 418B-04  
ISSUE J

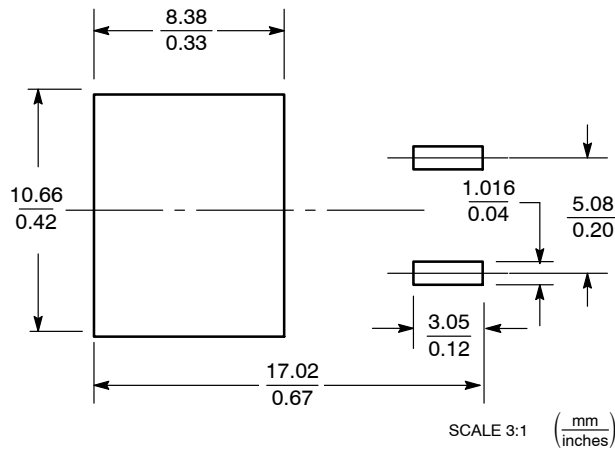


- NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.  
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100	BSC	2.54	BSC
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197	REF	5.00	REF
P	0.079	REF	2.00	REF
R	0.039	REF	0.99	REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40


- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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