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Renesas Electronics website: http://www.renesas.com

April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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#### **DATA SHEET**



### MOS FIELD EFFECT TRANSISTOR

#### NP100N055MDH, NP100N055NDH, NP100N055PDH

#### SWITCHING **N-CHANNEL POWER MOS FET**

#### **DESCRIPTION**

The NP100N055MDH, NP100N055NDH, NP100N055PDH are N-channel MOS Field Effect Transistors designed for high current switching applications.

#### ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP100N055MDH-S18-AY Note		Tube	TO-220 (MP-25K) typ. 1.9 g
NP100N055NDH-S18-AY Note		50 p/tube	TO-262 (MP-25SK) typ. 1.8 g
NP100N055PDH-E1-AY Note	Pure Sn (Tin)	Tape	
NP100N055PDH-E2-AY Note		800 p/reel	TO-263 (MP-25ZP) typ. 1.5 g

Note Pb-free (This product does not contain Pb in the external electrode.)

#### **FEATURES**

• Enhancing Tch(MAX.) to 200°C (Operation time until 250 Hr)

• Super low on-state resistance

- NP100N055MDH, NP100N055NDH

 $R_{DS(on)1} = 4.8 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A})$ 

 $R_{DS(on)2} = 6.6 \text{ m}\Omega \text{ MAX}. \text{ (Vgs} = 4.5 \text{ V, Ip} = 50 \text{ A)}$ 

- NP100N055PDH

 $R_{DS(on)1} = 4.4 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 50 \text{ A})$ 

 $R_{DS(on)2} = 6.2 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 4.5 \text{ V, ID} = 50 \text{ A)}$ 

- High avalanche energy, High avalanche current
- Logic level drive Type
- Low input capacitance

Ciss = 9500 pF TYP. (VDS = 25 V)

(TO-220)



(TO-262)





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#### ABSOLUTE MAXIMUM RATINGS $(T_A = 25^{\circ}C)$

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	VDSS	55	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±12	V
Drain Current (DC) (Tc = 25°C)	I <sub>D(DC)</sub>	±100	Α
Drain Current (pulse) (Tc = 25°C) Note1	I <sub>D(pulse)</sub>	±400	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	288	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch1</sub>	175	°C
Channel Temperature Note2	T <sub>ch2</sub>	200	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Repetitive Avalanche Current Note3	lar1	80	Α
Repetitive Avalanche Current Note4	I <sub>AR2</sub>	90	Α
Repetitive Avalanche Energy Note5	Ear	1000	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

2. Reliability test condition

High temperature bias condition ( $V_{DS}$  =  $V_{DSS}$ ,  $V_{GS}$  = 0 V, 250 Hr) High temperature gate bias condition ( $V_{DS}$  = 0 V,  $V_{GS}$  = 12 V, 250 Hr)

- **3.** L = 100 μH, Tch ≤ 200°C
- **4.** L = 10  $\mu$ H, Tch  $\leq$  200°C
- **5.** Tch  $\leq$  200°C, Rg = 25  $\Omega$ , Vgs = 12  $\rightarrow$  0 V

#### THERMAL RESISTANCE

<R>

Channel to Case Thermal Resistance	Rth(ch-C)	0.52	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	83.3	°C/W



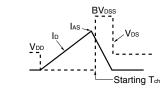
#### **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 55 V, V <sub>GS</sub> = 0 V			1	μΑ
Gate Leakage Current	Igss	V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0 V			±100	nA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance Note	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 50 A	45	95		S
Drain to Source On-state Resistance Note	RDS(on)1	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A NP100N055MDH, NP100N055NDH		3.8	4.8	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A NP100N055PDH		3.5	4.4	mΩ
	RDS(on)2	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 A NP100N055MDH, NP100N055NDH		4.6	6.6	mΩ
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 50 A NP100N055PDH		4.3	6.2	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 25 V,		9500	14000	pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V,		1000	1500	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		270	490	pF
Turn-on Delay Time	td(on)	V <sub>DD</sub> = 28 V, I <sub>D</sub> = 50 A,		24	53	ns
Rise Time	tr	V <sub>GS</sub> = 10 V,		11	28	ns
Turn-off Delay Time	td(off)	$R_G = 0 \Omega$		150	300	ns
Fall Time	tf			13	32	ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 44 V,		170	260	nC
Gate to Source Charge	QGS	V <sub>GS</sub> = 10 V,		29		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = 100 A		36		nC
Body Diode Forward Voltage Note	V <sub>F(S-D)</sub>	IF = 100 A, VGS = 0 V		0.93	1.5	V
Reverse Recovery Time	trr	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V,		60		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		120		nC

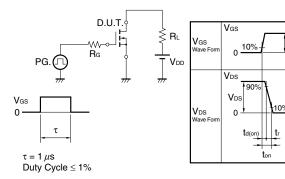
Note Pulsed

#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

# $R_{G} = 25 \Omega$ $PG. \square \leq 50 \Omega$ $V_{OS} = 12 \rightarrow 0 \text{ V}$ $W = 12 \rightarrow 0 \text{ V}$ $W = 12 \rightarrow 0 \text{ V}$



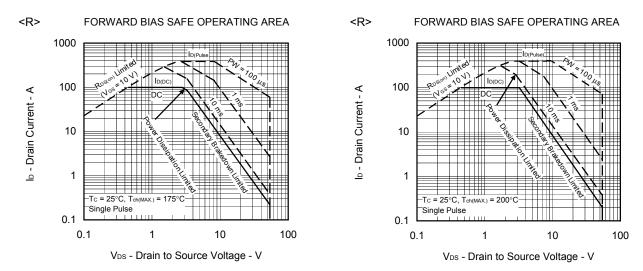
#### TEST CIRCUIT 2 SWITCHING TIME

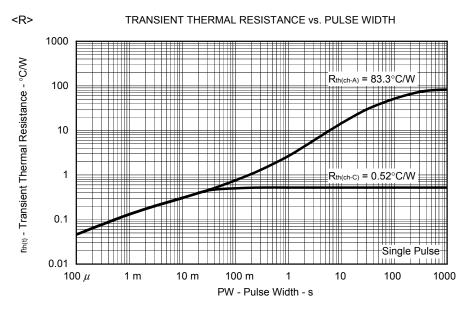


#### **TEST CIRCUIT 3 GATE CHARGE**



#### TYPICAL CHARACTERISTICS (TA = 25°C) (NP100N055MDH)



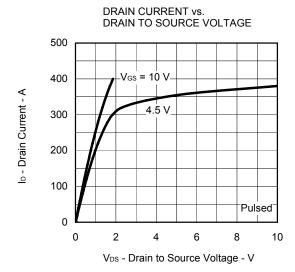


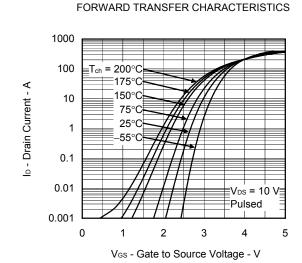
**Note** Confirm the operation tracks are in Safe Operating Area.



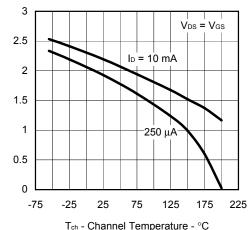
Ves(th) - Gate to Source Threshold Voltage - V

 $\mathsf{R}_{\mathsf{DS}(\varpi)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

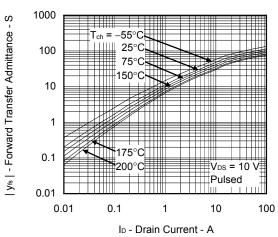




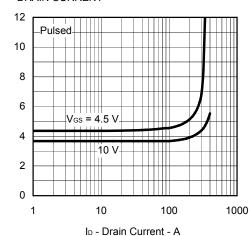
## GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



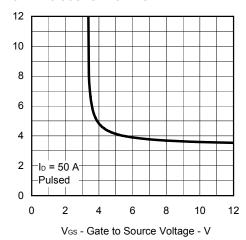
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



## DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



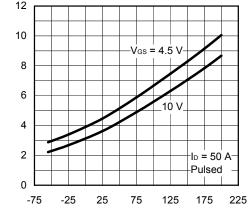
R<sub>DS(cn)</sub> - Drain to Source On-state Resistance - mΩ



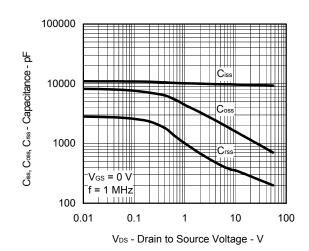
R<sub>DS(m)</sub> - Drain to Source On-state Resistance - mΩ



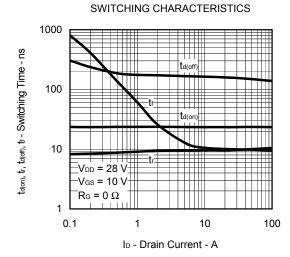
DRAIN TO SOURCE ON-STATE RESISTANCE vs.



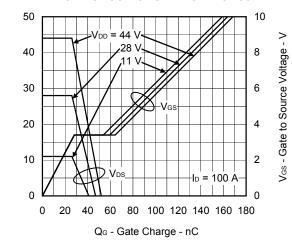
#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



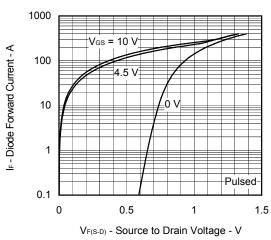
Tch - Channel Temperature - °C



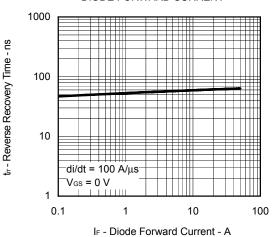
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



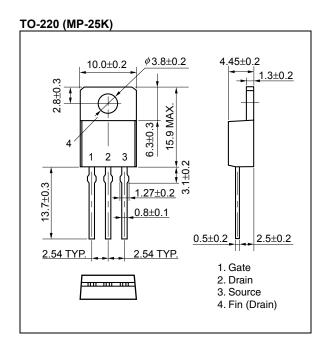
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

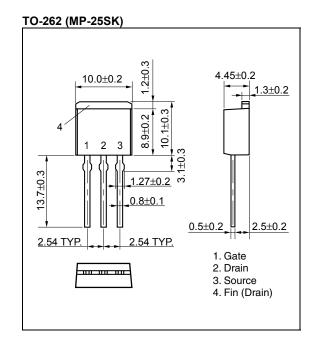


Vos - Drain to Source Voltage - V

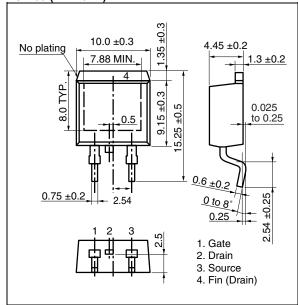


#### PACKAGE DRAWINGS (Unit: mm)

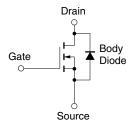




#### TO-263 (MP-25ZP)



#### **EQUIVALENT CIRCUIT**

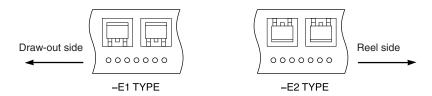


**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

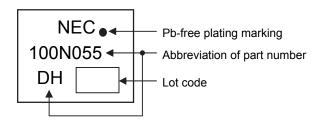


#### TAPE INFORMATION (NP100N055PDH)

There are two types (-E1, -E2) of taping depending on the direction of the device.



#### MARKING INFORMATION



#### RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the following recommended conditions.

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For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow NP100N055PDH	Maximum temperature (Package's surface temperature): 260°C or below Time at maximum temperature: 10 seconds or less Time of temperature higher than 220°C: 60 seconds or less Preheating time at 160 to 180°C: 60 to 120 seconds Maximum number of reflow processes: 3 times Maximum chlorine content of rosin flux (percentage mass): 0.2% or less	IR60-00-3
Wave soldering NP100N055MDH, NP100N055NDH	Maximum temperature (Solder temperature): 260°C or below Time: 10 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	THDWS
Partial heating NP100N055MDH, NP100N055NDH, NP100N055PDH	Maximum temperature (Pin temperature): 350°C or below Time (per side of the device): 3 seconds or less Maximum chlorine content of rosin flux: 0.2% (wt.) or less	P350

Caution Do not use different soldering methods together (except for partial heating).



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