

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# MOS FIELD EFFECT TRANSISTOR NP50P06SDG

## SWITCHING P-CHANNEL POWER MOSFET

### DESCRIPTION

The NP50P06SDG is P-channel MOS Field Effect Transistor designed for high current switching applications.

### ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP50P06SDG-E1-AY <sup>Note</sup>	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)
NP50P06SDG-E2-AY <sup>Note</sup>			

**Note** Pb-free (This product does not contain Pb in external electrode.)

### FEATURES

- Super low on-state resistance

$R_{DS(on)1} = 16.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -25 \text{ A)}$

$R_{DS(on)2} = 23.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -25 \text{ A)}$

- Low input capacitance

$C_{iss} = 5000 \text{ pF TYP.}$

(TO-252)



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	-60	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>c</sub> = 25°C)	I <sub>D(DC)</sub>	±50	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±150	A
Total Power Dissipation (T <sub>c</sub> = 25°C)	P <sub>T1</sub>	84	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.2	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to +175	°C
Single Avalanche Current <sup>Note2</sup>	I <sub>AS</sub>	32	A
<R> Single Avalanche Energy <sup>Note2</sup>	E <sub>AS</sub>	102	mJ

**Notes 1.** PW ≤ 10 μs, Duty Cycle ≤ 1%

**2.** Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = -30 V, R<sub>G</sub> = 25 Ω, V<sub>GS</sub> = -20 → 0 V

### THERMAL RESISTANCE

Channel to Case Thermal Resistance	R <sub>th(ch-C)</sub>	1.78	°C/W
Channel to Ambient Thermal Resistance	R <sub>th(ch-A)</sub>	125	°C/W

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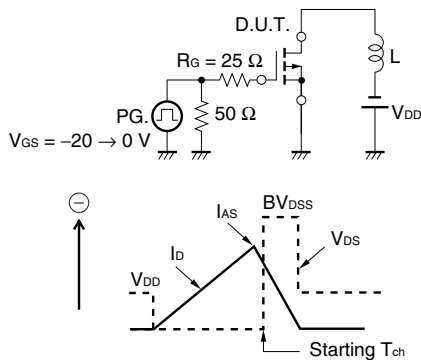
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**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)**

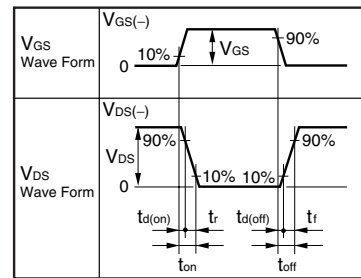
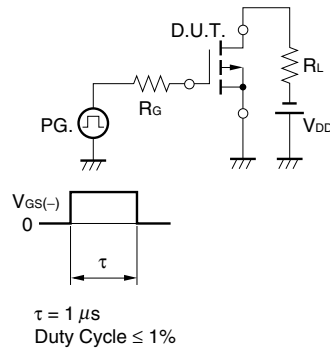
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V			-10	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±100	nA
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-1.0	-1.6	-2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -25 A	15	33		S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -25 A		13.2	16.5	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -25 A		14.9	23.0	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V,		5000		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V,		600		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		300		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -30 V, I <sub>D</sub> = -25 A,		13		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -10 V,		13		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 0 Ω		405		ns
Fall Time	t <sub>f</sub>			180		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -48 V,		100		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V,		11		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -50 A		30		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V		0.97	1.5	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V,		50		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = -100 A/μs		72		nC

**Note** Pulsed test PW ≤ 350 μs, Duty Cycle ≤ 2%

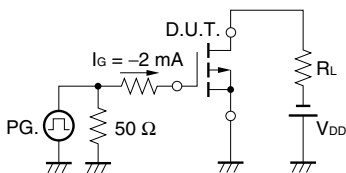
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



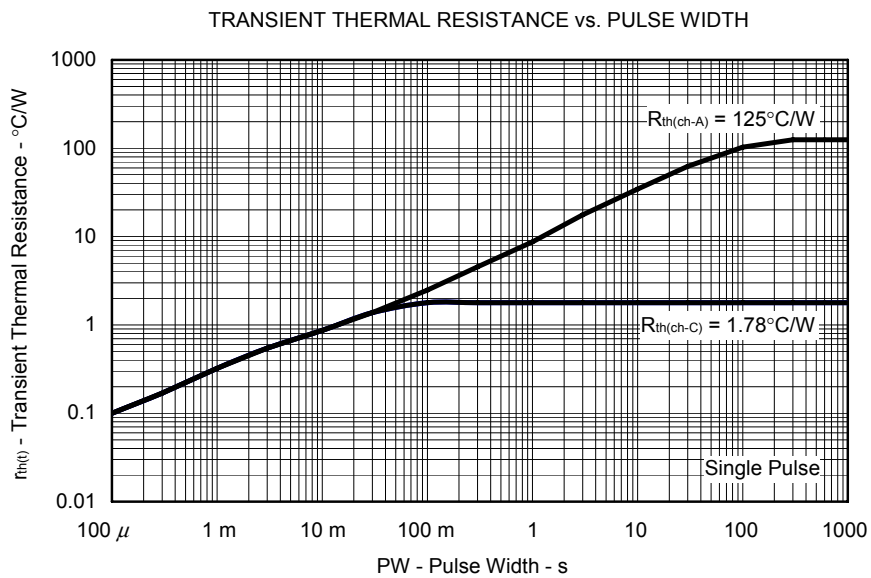
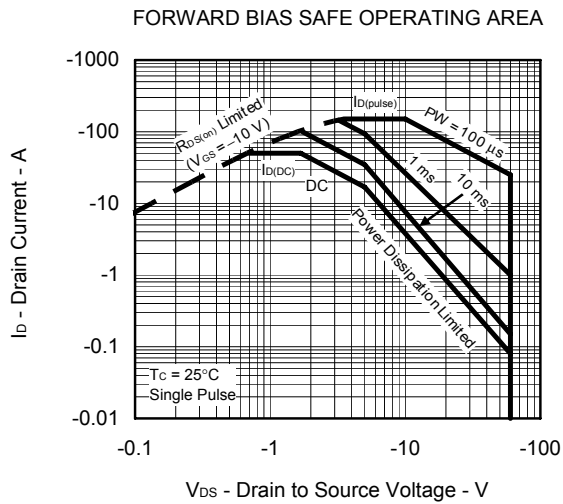
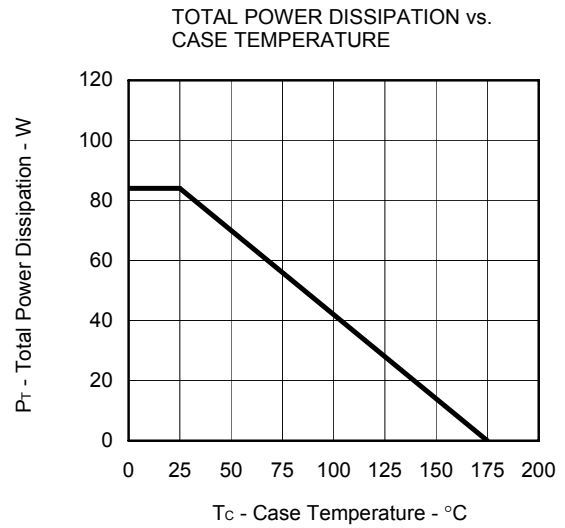
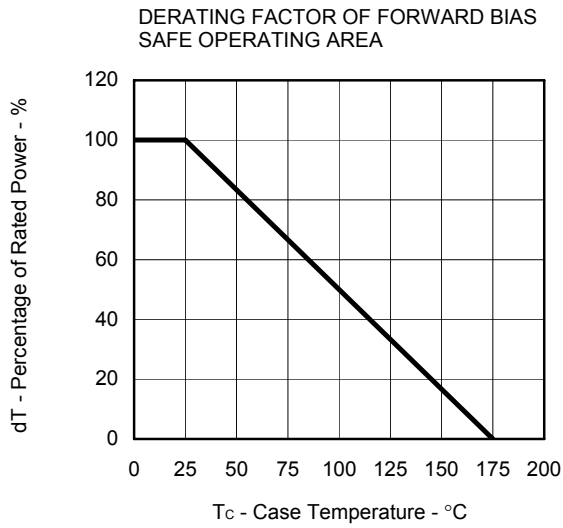
**TEST CIRCUIT 2 SWITCHING TIME**



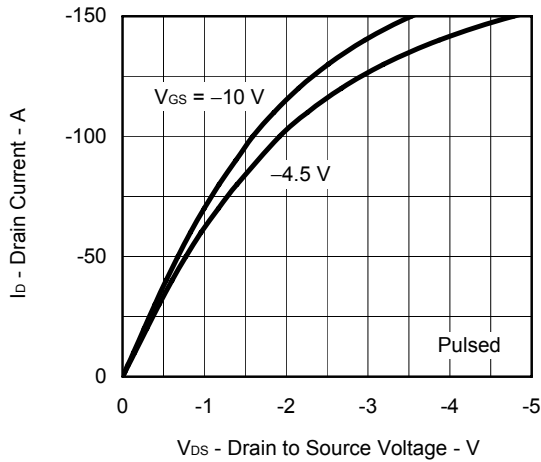
**TEST CIRCUIT 3 GATE CHARGE**



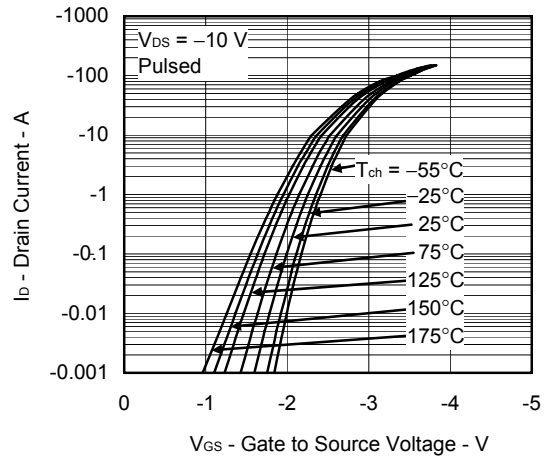
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)



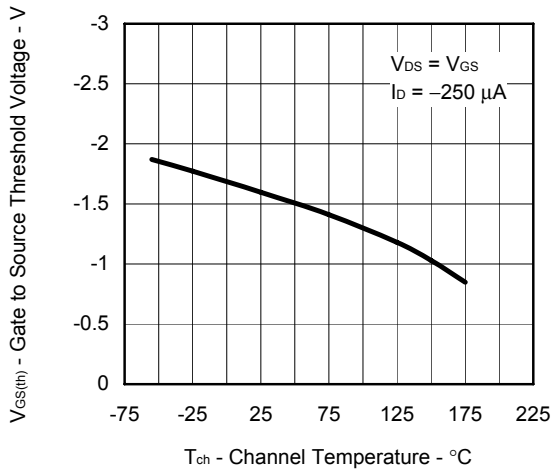
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



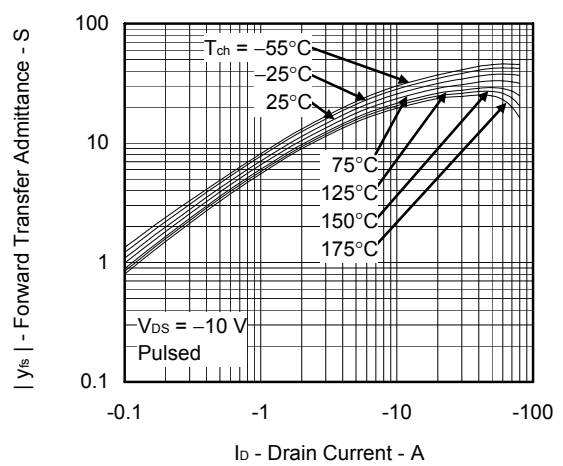
FORWARD TRANSFER CHARACTERISTICS



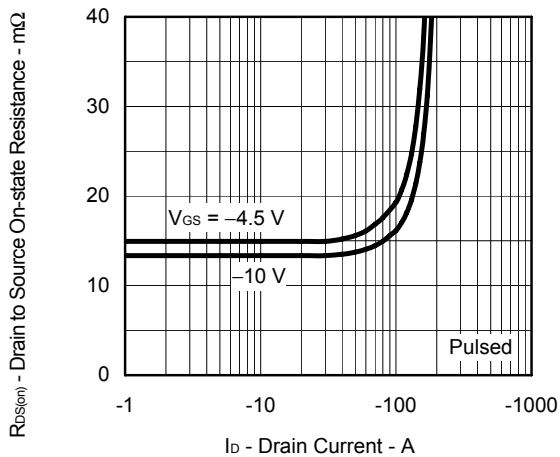
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



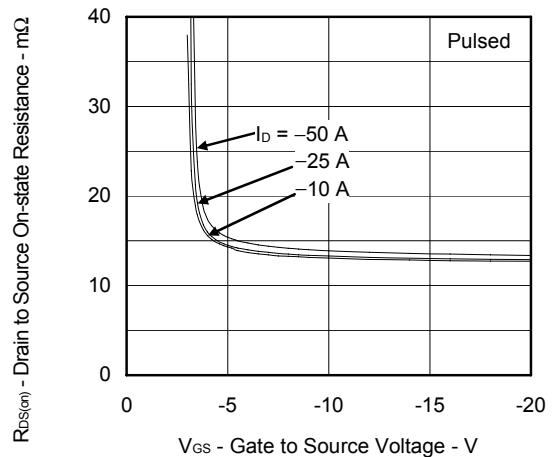
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



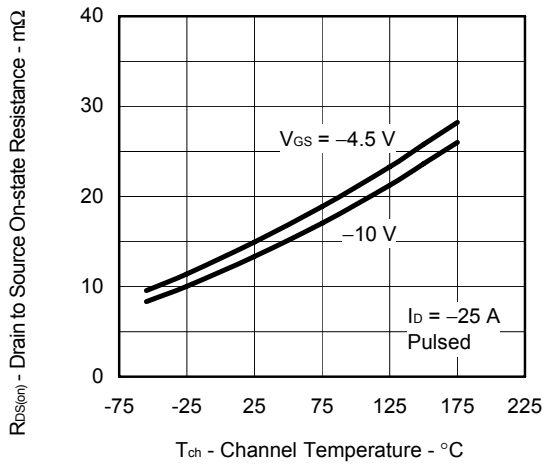
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



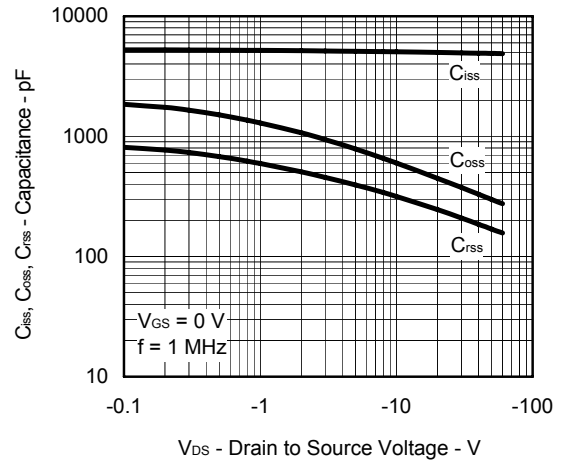
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



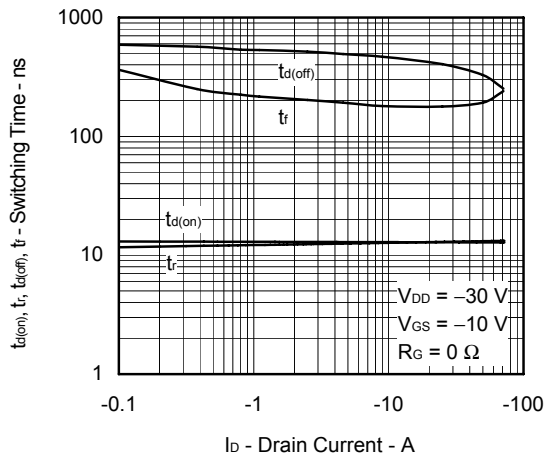
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



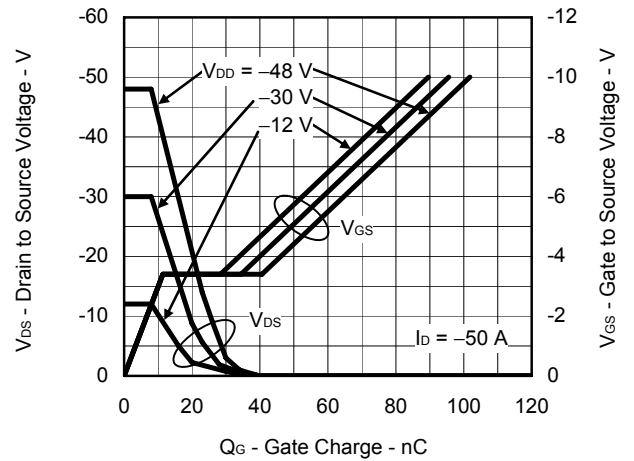
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



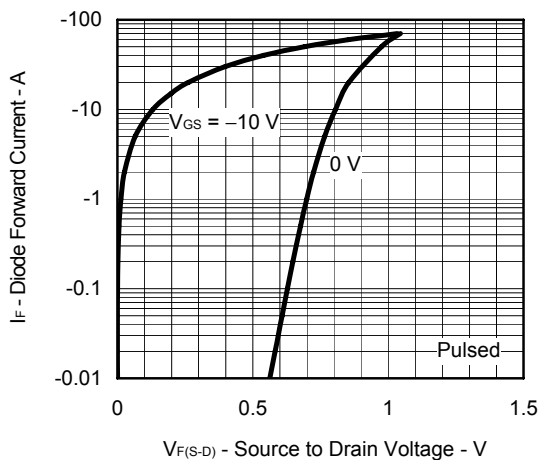
SWITCHING CHARACTERISTICS



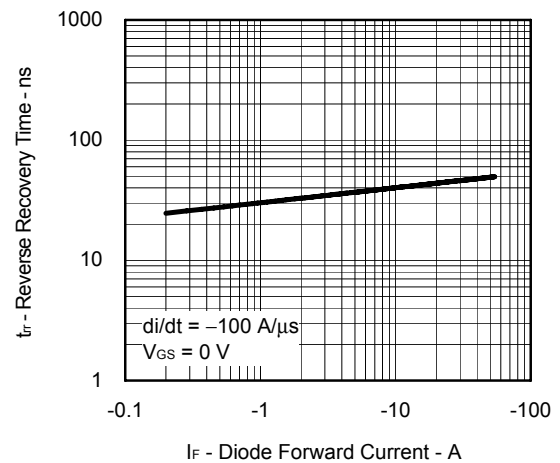
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

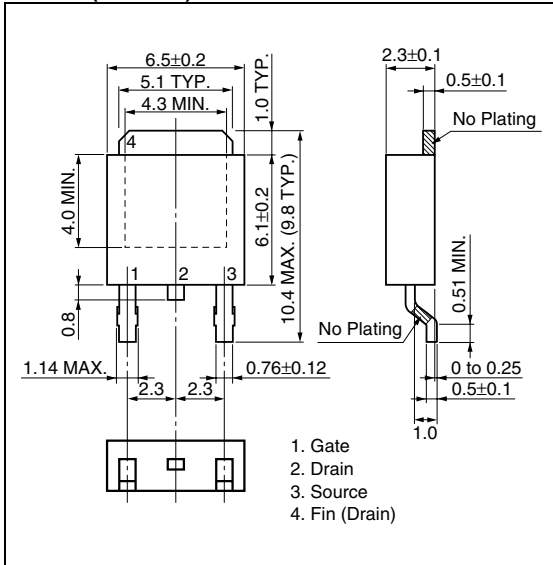


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

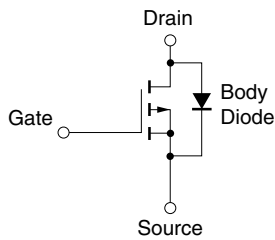


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.



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