

NP16N04YUG

MOS FIELD EFFECT TRANSISTOR

R07DS0362EJ0100 Rev.1.00 Jun 13, 2011

Description

The NP16N04YUG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
 - --- $R_{DS(on)}$ = 25 mΩ MAX. (V_{GS} = 10 V, I_D = 8 A)
- Low C_{iss} : $C_{iss} = 740 \text{ pF TYP}$. $(V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified
- Small size package 8-pin HSON

Ordering Information

Part No.	Lead Plating	Pac	Package	
NP16N04YUG-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP16N04YUG-E2-AY *1			Taping (E2 type)	

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	40	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±16	A
Drain Current (pulse) *1	I _{D(pulse)}	±48	A
Total Power Dissipation (T _C = 25°C)	P _{T1}	36	W
Total Power Dissipation (T _A = 25°C) *2	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *3	I _{AR}	13	A
Repetitive Avalanche Energy *3	E _{AR}	12	mJ

Thermal Resistance

Notes: *1. $T_C = 25^{\circ}C$, PW $\leq 10 \mu s$, Duty Cycle $\leq 1\%$

*2. Mounted on glass epoxy substrate of 40 mm x 40 mm x 1.6 mmt with 4% copper area (35 μ m)

*3. $T_{ch(peak)} \le 150^{\circ}C$, $R_G = 25 \Omega$

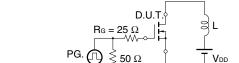
Caution This product is an electrostatic-sensitive device due to low ESD capability and should be handled with caution for electrostatic discharge. HBM (C = 100 pF, R = 1.5 k Ω) \pm 500 V.

Electrical Characteristics (T_A = 25°C)

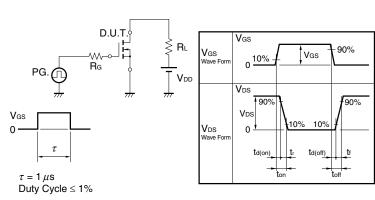
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I _{DSS}			1	μΑ	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I _{GSS}			±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$
Forward Transfer Admittance *1	y _{fs}	4	8		S	$V_{DS} = 5 \text{ V}, I_{D} = 8 \text{ A}$
Drain to Source On-state Resistance *1	R _{DS(on)}		20	25	mΩ	V _{GS} = 10 V, I _D = 8 A
Input Capacitance	C _{iss}		740	1110	pF	$V_{DS} = 25 V$,
Output Capacitance	Coss		83	110	pF	$V_{GS} = 0 V$,
Reverse Transfer Capacitance	C _{rss}		57	100	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		10	20	ns	$V_{DD} = 20 \text{ V}, I_D = 8 \text{ A},$
Rise Time	t _r		4	10	ns	V_{GS} = 10 V ,
Turn-off Delay Time	$t_{d(off)}$		19	38	ns	$R_G = 0 \Omega$
Fall Time	t _f		5	13	ns	
Total Gate Charge	Q_{G}		16	24	nC	$V_{DD} = 32 V$,
Gate to Source Charge	Q_{GS}		5		nC	$V_{GS} = 10 \text{ V},$
Gate to Drain Charge	Q_{GD}		6		nC	I _D = 16 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I _F = 16 A, V _{GS} = 0 V
Reverse Recovery Time	t _{rr}		25		ns	$I_F = 16 \text{ A}, V_{GS} = 0 \text{ V},$
Reverse Recovery Charge	Q _{rr}		24		nC	$di/dt = 100 A/\mu s$

Note: *1. Pulsed test

TEST CIRCUIT 1 AVALANCHE CAPABILITY



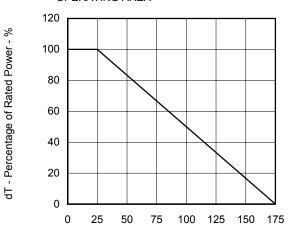
TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE

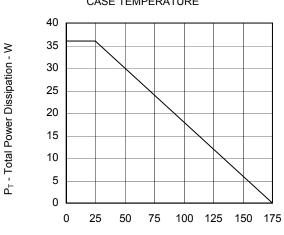
Typical Characteristics ($T_A = 25^{\circ}C$)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



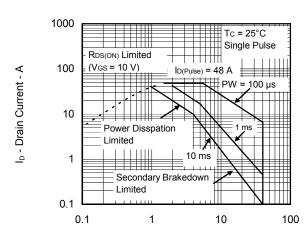
 T_{C} - Case Temperature - $^{\circ}\text{C}$

TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



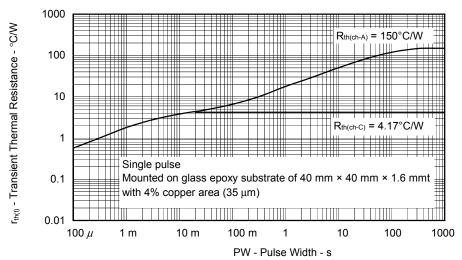
T_C - Case Temperature - °C

FORWARD BIAS SAFE OPERATING AREA



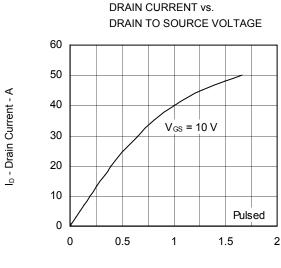
 $V_{\text{\scriptsize DS}}$ - Drain to Source Voltage - V

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

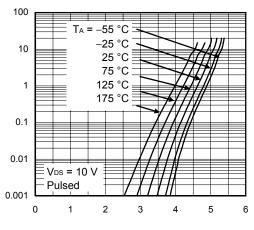


V_{GS(th)} - Gate to Source Threshold Voltage - V

 $R_{\text{DS}(\text{on})}$ - Drain to Source On-state Resistance - $m\Omega$







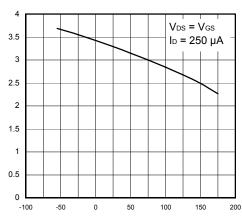
Ip - Drain Current - A

| y_{fs} | - Forward Transfer Admittance - S

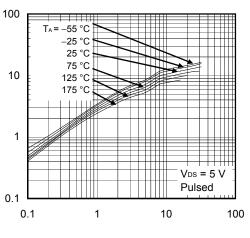
V_{DS} - Drain to Source Voltage - V

V_{GS} - Gate to Source Voltage - V





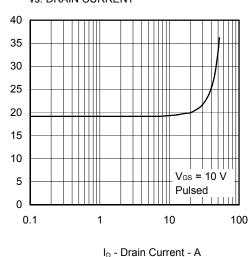
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



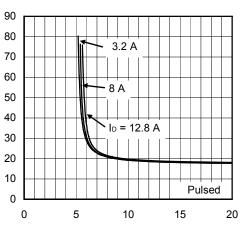
T_{ch} - Channel Temperature - °C

I_D - Drain Current - A

DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

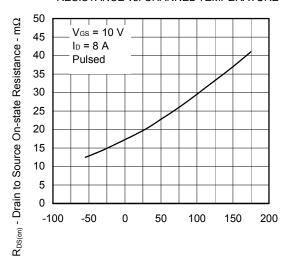


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



V_{GS} - Gate to Source Voltage - V

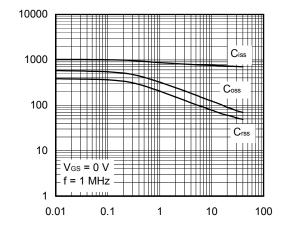
 $R_{\text{DS(on)}}$ - Drain to Source On-state Resistance - $m\Omega$



T_{ch} - Channel Temperature - °C

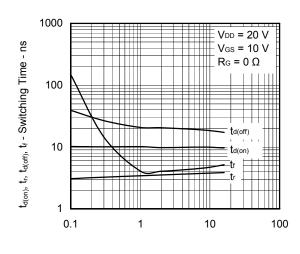
Ciss, Coss, Crss - Capacitance - pF

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



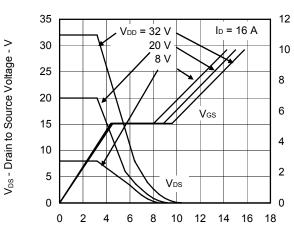
V_{DS} - Drain to Source Voltage - V

SWITCHING CHARACTERISTICS



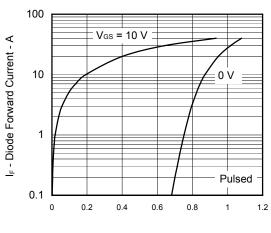
I_D - Drain Current - A

DYNAMIC INPUT/OUTPUT CHARACTERISTICS



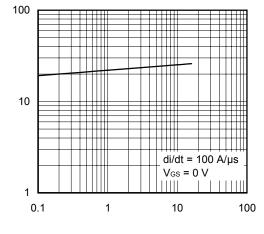
Q_G - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE



 $V_{\text{F(S-D)}}$ - Source to Drain Voltage - V

REVERSE RECOVERY TIME vs. DRAIN CURRENT

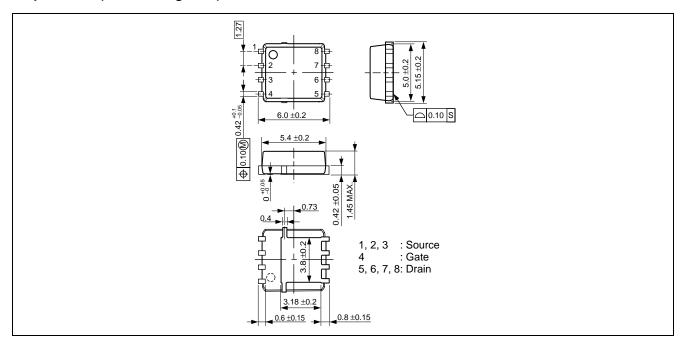


I_F - Drain Current - A

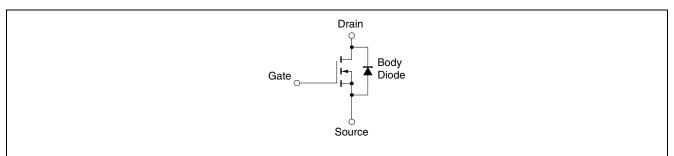
t_{rr} - Reverse Recovery Time - ns

Package Drawings (Unit: mm)

8-pin HSON (Mass: 0.13 g TYP.)



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History

NP16N04YUG Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Jun 13, 2011	_	First Edition Issued	

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