

September 1996 ADVANCE INFORMATION

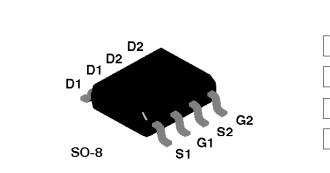
## NDS8961 Dual N-Channel Enhancement Mode Field Effect Transistor

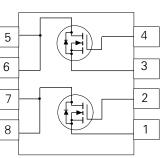
## **General Description**

SO-8 N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

## Features

- 3.1A, 30V.  $R_{DS(ON)} = 0.1\Omega @ V_{GS} = 10V R_{DS(ON)} = 0.15\Omega @ V_{GS} = 4.5V.$
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





## **Absolute Maximum Ratings** $T_A = 25^{\circ}C$ unless otherwise note

Symbol	Parameter	NDS8961	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
D	Drain Current - Continuous (Note 1a)	3.1	А
	- Pulsed	9	
PD	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
Γ <sub>J</sub> ,T <sub>stg</sub>	Operating and Storage Temperature Range	-55 to 150	°C
THERMA	AL CHARACTERISTICS		
R <sub>øja</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
R <sub>øJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

DSSZero Gate Voltage Drain Current $V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ $T_{J} = 55^{\circ}\text{C}$ 10 $\mu\text{A}$ GSSFGate - Body Leakage, Forward $V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$ 100nAGSSRGate - Body Leakage, Reverse $V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$ 100nAON CHARACTERISTICS (Note 2) $V_{OS} = V_{GS'} \text{ I}_D = 250 \ \mu\text{A}$ 13V $V_{GS(th)}$ Gate Threshold Voltage $V_{DS} = V_{GS'} \text{ I}_D = 250 \ \mu\text{A}$ 13V $R_{DS(ON)}$ Static Drain-Source On-Resistance $V_{GS} = 10 \text{ V}, \text{ I}_D = 3.1 \text{ A}$ 0.1 $\Omega$ $D(on)$ On-State Drain Current $V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$ 9A $V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$ 9AADIAN $V_{GS} = 4.5 \text{ V}, V_{DS} = 5 \text{ V}$ 1.3 AADIAN $V_{GS} = 0 \text{ V}, \text{ I}_S = 1.3 \text{ A}$ (Note 2)1.2 VVIdees:Idees:Idees:IdeesIdeesIdees	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Symbol	Parameter	Conditions		Min	Тур	Max	Units
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	LossZero Gate Voltage Drain Current $V_{0S} = 24$ V, $V_{0S} = 0$ VImage: Constraint of the state of the	OFF CHA	ARACTERISTICS						
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	$I_{DSS}$ Zero Gate Voltage Drain Current $V_{DS} = 24$ V, $V_{DS} = 0$ V $I_{J} = 55^{\circ}$ C $I_{J} = \mu \mu$ $I_{DSSF}$ Gate - Body Leakage, Forward $V_{DS} = 20$ V, $V_{DS} = 0$ V $I_{J} = 55^{\circ}$ C $I_{J} = 0$ $\mu$ $I_{DSSF}$ Gate - Body Leakage, Forward $V_{DS} = 20$ V, $V_{DS} = 0$ V $I_{J} = 0$ $\mu$ $I_{DO}$ ON CHARACTERISTICS (reare 2) $V_{DSS} = V_{DS}$ $I_{D} = 250$ $\mu$ $I_{J} = 31$ $A$ $0.1$ $\Omega$ $V_{DSSN}$ Static Drain-Source On-Resistance $V_{CS} = 10$ V, $I_{D} = 2.6$ $A$ $0.15$ $\Omega$ $I_{DOD}$ On-State Drain Current $V_{CS} = 10$ V, $V_{DS} = 5$ $V$ $9$ $A$ $V_{DS} = 45$ V, $V_{DS} = 5$ $V$ $4$ $A$ $\Omega$ $V_{DS} = 10$ V, $V_{DS} = 5$ $V$ $4$ $A$ $V_{DS} = 10$ V, $V_{DS} = 5$ $V$ $4$ $A$ $V_{DS} = 10$ V, $V_{DS} = 5$ $V$ $4$ $A$ $V_{DS} = 10$ V, $V_{DS} = 5$ $V$ $4$ $A$ $V_{DS} = 10$ V, $V_{DS} = 5$ $V$ $4$ $A$ $V_{DS} = 10$ V, $V_{DS} = 5$ $V$ $4$ $A$ $V_{DS} = 10$ V, $V_{DS} = 1.3$ A (bde $2$ ) $I_{LZ}$ $V$ VectorNotice Diobe ChARACTERISTICS AND MAXIMUM RATINGS $I_{S}$ Maximum Continuous Drain-Source Diode Forward Current $I_{LZ}$ $V$ $V_{DS} = 1.2$ $V$ $V_{SS} = 1.3$ A (bde $2$ ) $I_{LZ}$ $V$ VectorNote the pointed on a 0.02 in $P_{SS}$ of $20$ copper. $I_{S} = 1.3$ A (bde $2$ ) $I_{S} = 0$ $V$ $V_{S} = 0$ $V$ $I_{S} = 1.3$ A (bde $2$ ) $I_{S} = 0$ $V$ $V_{S} = 0$ $V$ $V_{S} = 0$ $V$ <td< th=""><th>BV<sub>DSS</sub></th><th>Drain-Source Breakdown Voltage</th><th><math>V_{GS} = 0 V, I_{D} = 250 \mu A</math></th><th></th><th>30</th><th></th><th></th><th>V</th></td<>	BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 V, I_{D} = 250 \mu A$		30			V
Image: constraint of the problem o	Image: Contract of the second sector contract.Image: Second sector contract the second sector contract of the second sector contract.1.3AA <t< td=""><td></td><td>Zero Gate Voltage Drain Current</td><td></td><td></td><td></td><td></td><td>1</td><td>μA</td></t<>		Zero Gate Voltage Drain Current					1	μA
$\begin{array}{ c c c c c c } \hline label{eq:loss} \hline la$	$\begin{array}{ c c c c c c } \hline label{eq:section} \hline label$	200			$T_{J} = 55^{\circ}C$			10	μA
$\begin{split} I_{GSSR} & Gate - Body Leakage, Reverse & V_{GS} = -20 V, V_{DS} = 0 V & -100 & nA \\ \hline ON CHARACTERISTICS (Note 2) \\ V_{GSIN} & Gate Threshold Voltage & V_{DS} = V_{GS'} I_D = 250 \mu\text{A} & 1 & 3 & V \\ \hline R_{DSION} & Static Drain-Source On-Resistance & V_{GS} = 10 V, I_D = 3.1 A & 0.1 & \Omega \\ \hline V_{GS} = 4.5 V, I_D = 2.6 A & 0.15 \\ \hline I_{Dom} & On-State Drain Current & V_{GS} = 10 V, V_{SS} = 5 V & 9 & A \\ \hline V_{GS} = 4.5 V, V_{SS} = 5 V & 4 & 0.15 \\ \hline DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS \\ \hline I_{S} & Maximum Continuous Drain-Source Diode Forward Current & 1.3 & A \\ \hline V_{SD} & Drain-Source Diode Forward Voltage & V_{GS} = 0 V, I_S = 1.3 A (Note 2) & 1.2 & V \\ \hline V_{HOE} & & & & & & & & & & & & & & & & & & &$	$\begin{array}{c ccccc} \hline C_{GSSR} & Gate - Body Leakage, Reverse & V_{GS} = -20 V, V_{DS} = 0 V & -100 & nA \\ \hline ON CHARACTERISTICS (Note 2) \\ \hline V_{GSHH} & Gate Threshold Voltage & V_{DS} = V_{GS'}, I_D = 250 \mu A & 1 & 3 & V \\ \hline V_{GS} = 10 V, I_D = 3.1 A & 0.1 & \Omega \\ \hline V_{GS} = 4.5 V, I_D = 2.6 A & 0.15 \\ \hline V_{GS} = 4.5 V, I_D = 2.6 A & 0.15 \\ \hline V_{GS} = 4.5 V, V_{OS} = 5 V & 9 & A \\ \hline Drain-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS \\ \hline I_{SO} & Drain-Source Diode Forward Voltage V_{GS} = 0 V, I_S = 1.3 A (Note 2) & 1.2 & V \\ \hline V_{SS} & Maximum Continuous Drain-Source Diode Forward Current & 1.3 & A \\ \hline V_{SD} & Drain-Source Diode Forward Voltage V_{GS} = 0 V, I_S = 1.3 A (Note 2) & 1.2 & V \\ \hline Mes: \\ \hline 1. R_{ack} is guaranteed by design while R_{ack} is determined by the user's board design. \\ \hline P_D(1) = \frac{T_{ack}}{T_{ack}} = \frac{T_{ack}}{T_{ack}} = I_D^2(1) \times R_{DS(ONET}, \\ \hline Typical R_{ack} for single device operation using the board layouts shown below on 4.5 x6° FR-4 PCB in a still air environment: \\ a. 78CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20 copper. \\ c. 130°CW when mounted on a 0.003 in' pad of 20$	GSSF	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	VGSBMGate Threshold Voltage $V_{DS} = V_{GS} \cdot I_{D} = 250 \ \mu A$ 13V $P_{DSOW}$ Static Drain-Source On-Resistance $V_{GS} = 10 \ V, \ I_{D} = 3.1 \ A$ 0.1 $\Omega$ $V_{GS} = 45 \ V, \ I_{D} = 2.6 \ A$ 0.15 $\Omega$ $I_{Dent}$ On-State Drain Current $V_{GS} = 45 \ V, \ V_{DS} = 5 \ V$ 9 $\Lambda$ <b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b> $I_{S}$ Maximum Continuous Drain-Source Diode Forward Current1.3 \ A $V_{SD}$ Drain-Source Diode Forward Voltage $V_{GS} = 0 \ V, \ I_{S} = 1.3 \ A$ $I_{Note 2I}$ 1.8 the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{v_{SD}}$ is guaranteed by design while $R_{w_{SD}}$ is determined by the user's board design. $P_{D}(0) = \frac{T_{er} - A_{er}}{R_{ex} I_{D}} = \frac{T_{er} - A_{er}}{R_{ex} I_{D}} = I_{D}^{-1} (0 \times R_{DSON)FT}$ .Typical $R_{u_{SD}}$ to ringle device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:a. 78°C/W when mounted on a 0.02 in* pad of 20c copper.b. 125°C/W when mounted on a 0.02 in* pad of 20c copper.c. 135°C/W when mounted on a 0.003 in* pad of 20c copper.c. 135°C/W when mounted on a 0.003 in* pad of 20c copper.c. 135°C/W when mounted on a 0.003 in* pad of 20c copper.c. 135°C/W when mounted on a 0.003 in* pad of 20c copper.c. 135°C/W when mounted on a 0.003 in* pad of 20c copper.c. 135°C/W when mounted on a 0.003 in* pad of 20c copper.Scale 1 : 1 on letter size paper.	1	Gate - Body Leakage, Reverse					-100	nA
$\begin{array}{ c c c c c c c c c c c c c c c c c c c$	RussionStatic Drain-Source On-Resistance $V_{GS} = 10 \text{ V}, I_{D} = 3.1 \text{ A}$ 0.10.10.1 $I_{Dom}$ On-State Drain Current $V_{GS} = 45 \text{ V}, I_{D} = 2.6 \text{ A}$ 0.150.15 <b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b> $I_S$ Maximum Continuous Drain-Source Diode Forward Current1.3A $V_{SD}$ Drain-Source Diode Forward Voltage $V_{GS} = 0 \text{ V}, I_S = 1.3 \text{ A}$ 1.2VNotes:1.1.3AA1.2V11.3A $V_{SD} = 5 \text{ V}$ 1.2VNotes:11.3A $V_{SD} = 1.3 \text{ A}$ Note 21.2VNotes:11.4 $V_{GS} = 0 \text{ V}, I_S = 1.3 \text{ A}$ Note 21.2VNotes:1.9 $U_{SD} = 0 \text{ V}, I_S = 1.3 \text{ A}$ Notes:1.9 $U_{SD} = 0.7 \text{ I}_S = 1.3 \text{ A}$ Notes:1.9 $U_{SD} = 0.7 \text{ I}_S = 1.3 \text{ A}$ Notes:1.9 $U_{SD} = 0.7 \text{ I}_S = 1.3 \text{ A}$ Notes:1.9 $U_{SD} = 0.7 \text{ I}_S = 1.3 \text{ A}$ Notes:1.9 $U_{SD} = 0.7 \text{ I}_S = 0.7 \text{ I}_S = 1.3 \text{ A}$ Note:1.9 $U_{SD} = 0.7 \text{ I}_S = 0.7 \text$	ON CHA	RACTERISTICS (Note 2)					•	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	ResolveStatic Drain-Source On-Resistance $V_{GS} = 10 \ V, \ I_D = 3.1 \ A$ 0.1 $\Omega$ $I_{Dom}$ On-State Drain Current $V_{GS} = 45 \ V, \ I_D = 2.6 \ A$ 0.15 $\Omega$ <b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b> $I_S$ Maximum Continuous Drain-Source Diode Forward Current1.3 \ A $V_{SS} = 45 \ V, \ V_{OS} = 5 \ V$ 41.2 \ V <b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b> $I_S$ Maximum Continuous Drain-Source Diode Forward Current1.3 \ A $V_{SO}$ Drain-Source Diode Forward Voltage $V_{CS} = 0 \ V, \ I_S = 1.3 \ A \ (Note 2)$ 1.2 \ VNotes:1. R <sub>Ain</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of th $P_{D}(0) = \frac{T_{brit}^T A}{R_{bac}(0)} = \frac{T_{brit}^T A}{R_{bac}(0)} = I_{b}^{-1}(0) \times R_{DS(M)0^T J}$ Typical R <sub>ain</sub> for single device operation using the board layouts shown below on 4.5*/5* TR-4 PCB in a still air environment:a. 78*CW when mounted on a 0.02 in* pad of 202 copper.b. 125*COW when mounted on a 0.02 in* pad of 202 copper.c. 135*COW when mounted on a 0.0103 in* pad of 202 copper.c. 135*COW when mounted on a 0.0003 in* pad of 202 copper.c. 135*COW when mounted on a 0.0003 in* pad of 202 copper.c. 135*COW when mounted on a 0.0003 in* pad of 202 copper.c. 135*COW when mounted on a 0.0003 in* pad of 202 copper.c. 135*COW when mounted on a 0.0003 in* pad of 202 copper.c. 135*COW when mounted on a 1.0003 in* pad of 202 copper.c. 135*COW when mounted on a 1.0003 in* pad of 202	V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS'}} I_{\text{D}} = 250 \ \mu\text{A}$		1		3	V
$\begin{array}{ c c c c c } \hline V_{GS} = 4.5 \ V, \ V_D = 2.6 \ A & 0.15 \\ \hline V_{GS} = 10 \ V, \ V_{DS} = 5 \ V & 9 & A \\ \hline V_{GS} = 10 \ V, \ V_{DS} = 5 \ V & 4 & A \\ \hline V_{GS} = 4.5 \ V, \ V_{DS} = 5 \ V & 4 & A \\ \hline \end{array}$	$V_{0S} = 4.5 \text{ V}, V_{0S} = 5.0  9  10  0.15  9  10  0.05  5.0  9  10  0.05  5.0  9  10  0.05  5.0  9  10  0.05  5.0  9  10  0.05  5.0  9  10  0.05  5.0  9  10  0.05  5.0  10  0.05  5.0  9  10  0.05  5.0  10  0.05  5.0  10  0.05  5.0  10  0.05  5.0  10  0.05  5.0  10  0.05  10  0.05  5.0  10  0.05  10  10  0.05  10 $		Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.1 A				0.1	Ω
Vas = 4.5 V, Vas = 5 V       4         DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS         Is       Maximum Continuous Drain-Source Diode Forward Current       1.3       A         Vsp       Drain-Source Diode Forward Voltage       Vas = 0 V, Is = 1.3 A (Note 2)       1.2       V         Nets:       1.3       A       A       Integration of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of th drain pins. Rac is guaranteed by design while Rac is determined by the user's board design.       Pp(t) = T_{J-TA}^{J-TA} = T_{A_{act}AB_{act}}^{J-TA} = I_{0}^{J-TA} = I_{0}^{J-T	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5 V       4         DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS         Is       Maximum Continuous Drain-Source Diode Forward Current       1.3       A         V <sub>S0</sub> Drain-Source Diode Forward Voltage       V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A (Note 2)       1.2       V         Notes:       1.       1.3       A       A       A         1. 8. us is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{uc}$ is guaranteed by design while $R_{wch}$ is determined by the user's board design. $P_D(0) = \frac{T_p - T_A}{T_{mA}} = \frac{T_p - T_A}{R_{uc} - R_{uc} - T_p^{-1} A_{uc}} = I_D^2(t) \times R_{DS(ON) \oplus T_J}$ Typical $R_{ua}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:       a. 78"CM when mounted on a 0.02 in <sup>2</sup> pad of 202 copper.         a. 138"CCW when mounted on a 0.02 in <sup>2</sup> pad of 202 copper.       135"CCW when mounted on a 0.003 in <sup>2</sup> pad of 202 copper.       135"CCW when mounted on a 0.003 in <sup>2</sup> pad of 202 copper.         a. 138"CCW when mounted on a 0.003 in <sup>2</sup> pad of 202 copper.       135"CCW when mounted on a 0.003 in <sup>2</sup> pad of 202 copper.       10       Image: Comparison of the diate comparison of the diat for the dia			$V_{GS} = 4.5 \text{ V}, \ I_{D} = 2.6 \text{ A}$				0.15	
V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5 V       4         DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS         Is       Maximum Continuous Drain-Source Diode Forward Current       1.3       A         V <sub>SD</sub> Drain-Source Diode Forward Voltage       V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A (Note 2)       1.2       V         Notes:         1. R <sub>but</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of th drain pins. R <sub>buc</sub> is guaranteed by design while R <sub>buc</sub> is determined by the user's board design.       P <sub>D</sub> (t) = $\frac{T_{br}T_A}{R_{but}00} = \frac{T_{br}T_A}{R_{but}00} = I_D^2(t) \times R_{DS(ON)@TJ}$ Typical R <sub>buc</sub> respective to a 0.02 in <sup>2</sup> pad of 2oz copper.         b. 125 CW when mounted on a 0.02 in <sup>2</sup> pad of 2oz copper.         c. 135°CW when mounted on a 0.03 in <sup>2</sup> pad of 2oz copper.         Coppertion using the board layouts shown below on 4.5*x5° FR-4 PCB in a still air environment:         a. 78°CW when mounted on a 0.003 in <sup>2</sup> pad of 2oz copper.         c. 135°CW when mounted on a 0.003 in <sup>2</sup> pad of 2oz copper.         Compone:         Compone:         Compone:         Compone:         Compone:         Compone:         Compone:         C	$V_{CS} = 4.5 V, V_{DS} = 5 V$ 4DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS $I_S$ Maximum Continuous Drain-Source Diode Forward Current1.3A $V_{SD}$ Drain-Source Diode Forward Voltage $V_{GS} = 0.V, I_S = 1.3 A$ (Note 2)1.2VNotes:1. R <sub>ax</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{wc}$ is guaranteed by design while $R_{wcA}$ is determined by the user's board design. $P_D(0) = \frac{T_{wcTA}}{T_{max}} = \frac{T_{wcTA}}{R_{wcA}} = I_D^{-1}(t) \times R_{DS(ON)@TJ}$ Typical $R_{wA}$ for single device operation using the board layouts shown below on 4.5'x5' FR-4 PCB in a still air environment:a. 78'CW when mounted on a 0.02 in' pad of 202 copper.b. 125'CW when mounted on a 0.003 in' pad of 202 copper.137'CW when mounted on a 0.003 in' pad of 202 copper.colspan="2">1010OUT in pad of 202 copper.colspan="2">137'CW when mounted on a 0.003 in' pad of 202 copper.Colspan="2">1010Colspan="2">Colspan="2"Colspan="2"Colspan="2"Colspan="2"Colspan="2"Colspan="	D(on)	On-State Drain Current	$V_{\rm GS}=10~V,~V_{\rm DS}=5~V$		9			А
J       Drain-Source Diode Forward Voltage $V_{GS} = 0$ V, $I_S = 1.3$ A (Note 2)       1.2       V         Notes:       1. $R_{uA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of th drain pins. $R_{uS}$ is guaranteed by design while $R_{uSA}$ is determined by the user's board design. $P_D(t) = \frac{T_2 - T_A}{R_{uA}(0)} = I_D^2(t) \times R_{DS(0N) \oplus T_J}$ Typical $R_{uA}$ for single device operation using the board layouts shown below on 4.5 "x5" FR-4 PCB in a still air environment:       a. 78°C/W when mounted on a 0.02 in² pad of 2oz copper.         b. 125°CW when mounted on a 0.003 in² pad of 2oz copper.       c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.004 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.005 in² pad of 2oz copper.       f         diamond in a 0.005 in² pad of 2oz copper.       f         diamond in a 0.005 in² pad of 2oz copper.       f	Is       Maximum Continuous Drain-Source Diode Forward Current       1.3       A $V_{5D}$ Drain-Source Diode Forward Voltage $V_{6S} = 0 V$ , $I_{S} = 1.3 A$ (Note 2)       1.2       V         Notes:       1.8       as the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain prins. $R_{uc}$ is guaranteed by design while $R_{uc}$ is determined by the user's board design. $P_0(0) = \frac{T_a - T_A}{R_{uk} 0} = \frac{T_a - T_A}{R_{uc} + R_{uc} A_0} = f_0^2(0) \times R_{D(0N)@T_J}$ Typical $R_{uc}$ the case operation using the board layouts shown below on 4.5*x5* FR-4 PCB in a still air environment:       a. 78°CW when mounted on a 0.02 in <sup>2</sup> pad of 2oz copper.         b. 125°CW when mounted on a 0.02 in <sup>2</sup> pad of 2oz copper.       c. 135°CW when mounted on a 0.03 in <sup>2</sup> pad of 2oz copper.       1         c. 135°CW when mounted on a 0.03 in <sup>2</sup> pad of 2oz copper.       1       1       1         c. 135°CW when mounted on a 0.03 in <sup>2</sup> pad of 2oz copper.       1       1       1         c. 135°CW when mounted on a 0.03 in <sup>2</sup> pad of 2oz copper.       1       1       1       1         discussion       0       0       1       0       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1       1			$V_{\text{GS}} = 4.5 \text{ V},  \text{V}_{\text{DS}} = 5 \text{ V}$		4			
J       Drain-Source Diode Forward Voltage $V_{GS} = 0$ V, $I_S = 1.3$ A (Note 2)       1.2       V         Notes:       1. $R_{uA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of th drain pins. $R_{uS}$ is guaranteed by design while $R_{uSA}$ is determined by the user's board design. $P_D(t) = \frac{T_2 - T_A}{R_{uA}(0)} = I_D^2(t) \times R_{DS(0N) \oplus T_J}$ Typical $R_{uA}$ for single device operation using the board layouts shown below on 4.5 "x5" FR-4 PCB in a still air environment:       a. 78°C/W when mounted on a 0.02 in² pad of 2oz copper.         b. 125°CW when mounted on a 0.003 in² pad of 2oz copper.       c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.003 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.004 in² pad of 2oz copper.       f         c. 135°CW when mounted on a 0.005 in² pad of 2oz copper.       f         diamond in a 0.005 in² pad of 2oz copper.       f         diamond in a 0.005 in² pad of 2oz copper.       f	3       Drain-Source Diode Forward Voltage $V_{GS} = 0$ V, $I_S = 1.3$ A (Note 2)       1.2       V         Notes:       1. $R_{ux}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{ux}$ is guaranteed by design while $R_{ux}$ is determined by the user's board design. $P_D(t) = \frac{T_a T_a}{R_{ux} (t)} = \frac{T_b T_a}{R_{ux} (t)} = I_D^2(t) \times R_{DS(ON) \otimes T_d}$ Typical $R_{ux}$ for single device operation using the board layouts shown below on 4.5°x5° FR-4 PCB in a still air environment:       a. 78°C/W when mounted on a 0.02 in² pad of 2oz copper.         b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.       c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.         c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.       10         c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.       10         c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.       10         c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.       10         c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.       10         c. 135°C/W when mounted on a 0.004 in² pad information the solder mounter information th	DRAIN-S	OURCE DIODE CHARACTERIST	ICS AND MAXIMUM RA	TINGS	_			_
Notes: 1. $R_{axa}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of th drain pins. $R_{axc}$ is guaranteed by design while $R_{aca}$ is determined by the user's board design. $P_{D}(t) = \frac{T_{v}-T_{A}}{R_{au}A(1)} = \frac{T_{v}-T_{A}}{R_{au}C+R_{aca}(0)} = I_{D}^{2}(t) \times R_{DS(ON) \oplus T_{J}}$ Typical $R_{u,A}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment: a. 78°CW when mounted on a 0.05 in <sup>2</sup> pad of 2oz copper. b. 125°CW when mounted on a 0.003 in <sup>2</sup> pad of 2oz copper. c. 135°CW when mounted on a 0.003 in <sup>2</sup> pad of 2oz copper. 10 10 10 10 10 10 10 10 10 10	Notes: 1. $R_{uxh}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{uxc}$ is guaranteed by design while $R_{uch}$ is determined by the user's board design. $P_D(t) = \frac{T_a - T_A}{R_{uxc} H_{uxc} (th)} = \frac{T_a - T_A}{R_{ux} + R_{uxc} (th)} = I_D^2(t) \times R_{DS(ON) \otimes T_A}$ Typical $R_{uxh}$ for single device operation using the board layouts shown below on 4.5°x5° FR-4 PCB in a still air environment: a. 78°C/W when mounted on a 0.02 in <sup>2</sup> pad of 2oz copper. b. 125°C/W when mounted on a 0.02 in <sup>2</sup> pad of 2oz copper. c. 135°C/W when mounted on a 0.003 in <sup>2</sup> pad of 2oz copper. c. 135°C/W when mounted on a 0.003 in <sup>2</sup> pad of 2oz copper. Scale 1 : 1 on letter size paper.	s	Maximum Continuous Drain-Source	Diode Forward Current				1.3	А
<ul> <li>1. R<sub>exa</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>exc</sub> is guaranteed by design while R<sub>exc</sub> is determined by the user's board design.</li> <li>P<sub>D</sub>(t) = <sup>T<sub>y</sub>-T<sub>A</sub></sup>/<sub>R<sub>ext</sub>(t)</sub> = <sup>T<sub>y</sub>-T<sub>A</sub></sup>/<sub>R<sub>ext</sub>(t)</sub> = l<sup>2</sup><sub>D</sub>(t)×R<sub>DS(ON)@T<sub>J</sub></sub></li> <li>Typical R<sub>uxA</sub> for single device operation using the board layouts shown below on 4.5*x5" FR-4 PCB in a still air environment:</li> <li>a. 78°CW when mounted on a 0.05 in<sup>2</sup> pad of 2oz copper.</li> <li>b. 125°CW when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.</li> <li>c. 135°CW when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.</li> <li>difference of the still air environment of the still air environment.</li> <li>a. 78°CW when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.</li> <li>b. 125°CW when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.</li> <li>c. 135°CW when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.</li> <li>difference of the still air environment.</li> <li>e. 135°CW when mounted on a 0.003 in<sup>2</sup> pad of 2oz copper.</li> <li>f) the still air environment.</li> <li>f) the still air environment.</li> <li>f) the still air environment.</li> <li>g) the still air envine still air environment.</li> <li>g) the still ai</li></ul>	1. $R_{uch}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{uch}$ is guaranteed by design while $R_{uch}$ is determined by the user's board design. $P_D(t) = \frac{T_2 - T_A}{R_{uch} 0} = \frac{T_2 - T_A}{R_{uch} 0} = l_D^2(t) \times R_{DS(0N)@T_A}$ Typical $R_{uch}$ for single device operation using the board layouts shown below on 4.5°x5° FR-4 PCB in a still air environment: a. 78°CW when mounted on a 0.02 in <sup>2</sup> pad of 2oz copper. b. 125°CW when mounted on a 0.003 in <sup>2</sup> pad of 2oz copper. c. 135°CW when mounted on a 0.003 in <sup>2</sup> pad of 2oz copper. The formation of the formatio	$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V, I_{S} = 1.3 A$ (Note 2)				1.2	V
	Scale 1: 1 on letter size paper.	1. $R_{eJA}$ is the drain pins $P_D(t) = \frac{T}{R}$ Typical $R_{e}$ a.	$\begin{array}{l} R_{\text{euc}} \text{ is guaranteed by design while } R_{\text{ecA}} \text{ is determine} \\ \frac{\Gamma_J - \Gamma_A}{R_{\text{eJC}} + R_{\text{eCA}}(t)} = \frac{\Gamma_J - \Gamma_A}{R_{\text{eJC}} + R_{\text{eCA}}(t)} = I_D^2(t) \times R_{\text{DS(ON)} \oplus \text{T}_J} \\ \frac{\Gamma_J}{R_{\text{eJC}} + R_{\text{eCA}}(t)} = I_D^2(t) \times R_{\text{DS(ON)} \oplus \text{T}_J} \\ \frac{\Gamma_J}{R_{\text{eJC}} + R_{\text{eCA}}(t)} = I_D^2(t) \times R_{\text{DS(ON)} \oplus \text{T}_J} \\ \frac{\Gamma_J}{R_{\text{eJC}} + R_{\text{eCA}}(t)} = I_D^2(t) \times R_{\text{DS(ON)} \oplus \text{T}_J} \\ \frac{\Gamma_J}{R_{\text{eJC}} + R_{\text{eCA}}(t)} = I_D^2(t) \times R_{\text{DS(ON)} \oplus \text{T}_J} \\ \frac{\Gamma_J}{R_{\text{eJC}} + R_{\text{eCA}}(t)} = I_D^2(t) \times R_{\text{DS(ON)} \oplus \text{T}_J} \\ \frac{\Gamma_J}{R_{\text{eJC}} + R_{\text{eCA}}(t)} = I_D^2(t) \times R_{\text{DS(ON)} \oplus \text{T}_J} \\ \frac{\Gamma_J}{R_{\text{eCA}}(t)} = I_D^2(t) \times R_{\text{ECA}}(t) \times R_{\text{ECA}}(t) $	d by the user's board design. s shown below on 4.5"x5" FR-4 PCB in a per.			solder mo	unting surfa	ace of the
Scale 1 : 1 on letter size paper.		1. $R_{a_{JA}}$ is the drain pins $P_D(t) = \frac{1}{R}$ Typical $R_a$ a. b.	$\begin{array}{l} R_{\text{Buc}} \text{ is guaranteed by design while } R_{\text{BcA}} \text{ is determine} \\ \frac{T_J - T_A}{R_{\text{BLA}}(t)} = \frac{T_J - T_A}{R_{\text{BCA}}(t)} = I_D^2(t) \times R_{\text{DS}(\text{ON}) \otimes T_J} \\ R_{\text{BLA}} \text{ for single device operation using the board layouts} \\ 78^\circ\text{C/W} \text{ when mounted on a 0.5 in}^2 \text{ pad of 2oz copp} \\ 125^\circ\text{C/W} \text{ when mounted on a 0.02 in}^2 \text{ pad of 2oz cord} \\ 135^\circ\text{C/W} \text{ when mounted on a 0.003 in}^2 \text{ pad of 2oz cord} \\ \end{array}$	d by the user's board design. s shown below on 4.5"x5" FR-4 PCB in a per. opper. copper.			solder mo	unting surfa	ace of the
	2. Pulse Test: Pulse Width $\leq$ 300µs, Duty Cycle $\leq$ 2.0%.	1. $R_{a_{JA}}$ is the drain pins $P_D(t) = \frac{1}{R}$ Typical $R_a$ a. b.	$\begin{array}{c} R_{euc} \text{ is guaranteed by design while } R_{ecA} \text{ is determine} \\ \frac{\Gamma_J - \Gamma_A}{R_{euC} + R_{ecA}(t)} = I_D^2(t) \times R_{DS(ON) \oplus T_J} \\ R_{euA}(t) = \frac{T_J - T_A}{R_{euC} + R_{ecA}(t)} = I_D^2(t) \times R_{DS(ON) \oplus T_J} \\ R_{euA}(t) = R_{euC} + R_{ecA}(t) = I_D^2(t) \times R_{DS(ON) \oplus T_J} \\ R_{euA}(t) = R_{euC} + R_{ecA}(t) = R_{euA}(t) \times R_{DS(ON) \oplus T_J} \\ R_{euA}(t) = R_{EuA}(t)$	ad by the user's board design. s shown below on 4.5"x5" FR-4 PCB in a ber. copper. b b	still air environment	: ^^? }}	φ. <i>ο</i> 11	unting surfa	ace of the
	2. Puise Test: Puise vitatn $\leq$ 300µs, Duty Cycle $\leq$ 2.0%.	1. $R_{aJA}$ is the drain pins $P_D(t) = \frac{1}{R}$ Typical $R_a$ a. b. c.	$\begin{array}{c} R_{euc} \text{ is guaranteed by design while } R_{ecA} \text{ is determine} \\ \frac{\Gamma_J - \Gamma_A}{R_{elA}(1)} = \frac{T_J - T_A}{R_{elA}(1)} = I_D^2(1) \times R_{DS(ON)@T_J} \\ \frac{\Gamma_J}{R_{elA}(1)} = \frac{T_J - T_A}{R_{elA}(1)} = I_D^2(1) \times R_{DS(ON)@T_J} \\ \frac{\Gamma_J}{R_{elA}(1)} = \frac{\Gamma_J}{R_{elA}(1)} \times R_{DS(ON)@T_J} \\ \frac{\Gamma_J}{R_{elA}(1)} \times R_{DS(ON)@T_J} \\ \frac{\Gamma_J}{R_{elA}(1)} = \frac{\Gamma_J}{R_{elA}(1)} \times R_{DS(ON)@T_J} \\ \frac{\Gamma_J}{R_{e$	ad by the user's board design. s shown below on 4.5"x5" FR-4 PCB in a ber. copper. b b	still air environment	: ^^? }}	φ. <i>ο</i> 11	unting surfa	ace of the
		1. $R_{aJA}$ is the drain pins $P_D(t) = \frac{1}{R}$ Typical $R_a$ a. b. c.	$\begin{array}{c} R_{eac} \text{ is guaranteed by design while } R_{ecA} \text{ is determine} \\ r_J-T_A = \frac{T_J-T_A}{R_{eJC}+R_{eCA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = \frac{T_J-T_A}{R_{eJC}+R_{eCA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{eCA}(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{EA}(t) \times R_{DS}(t) \\ r_{BalC}(t) = r_{BalC}+R_{EA}(t) \times R_{DS}(t)$	ad by the user's board design. s shown below on 4.5"x5" FR-4 PCB in a ber. copper. b b	still air environment	: ^^? }}	φ. <i>ο</i> 11	unting surfa	ace of the
		1. $R_{aJA}$ is the drain pins $P_D(t) = \frac{1}{R}$ Typical $R_a$ a. b. c.	$\begin{array}{c} R_{eac} \text{ is guaranteed by design while } R_{ecA} \text{ is determine} \\ r_J-T_A = \frac{T_J-T_A}{R_{eJC}+R_{eCA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = \frac{T_J-T_A}{R_{eJC}+R_{eCA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{eCA}(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{EA}(t) \times R_{DS}(t) \\ r_{BalC}(t) = r_{BalC}+R_{EA}(t) \times R_{DS}(t)$	ad by the user's board design. s shown below on 4.5"x5" FR-4 PCB in a ber. copper. b b	still air environment	: ^^? }}	φ. <i>ο</i> 11	unting surfa	ace of the
		1. $R_{auA}$ is the drain pins $P_D(t) = \frac{1}{R}$ Typical $R_a$ a. b. c.	$\begin{array}{c} R_{eac} \text{ is guaranteed by design while } R_{ecA} \text{ is determine} \\ r_J-T_A = \frac{T_J-T_A}{R_{eJC}+R_{eCA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = \frac{T_J-T_A}{R_{eJC}+R_{eCA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalA}(t) = r_{BalC}+R_{eCA}(t) = I_D^2(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{eCA}(t) \times R_{DS(ON)@T_J} \\ r_{BalC}(t) = r_{BalC}+R_{EA}(t) \times R_{DS}(t) \\ r_{BalC}(t) = r_{BalC}+R_{EA}(t) \times R_{DS}(t)$	ad by the user's board design. s shown below on 4.5"x5" FR-4 PCB in a ber. copper. b b	still air environment	: ^^? }}	φ. <i>ο</i> 11	unting surfa	ace of the