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ADVANCE INFORMATION

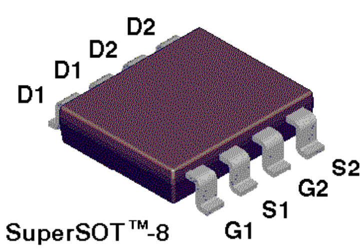
NDH8504P
Dual P-Channel Enhancement Mode Field Effect Transistor

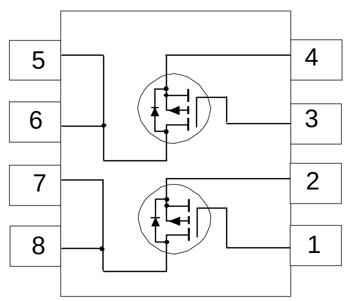
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -2.5A, -30V. $R_{DS(ON)} = 0.08\Omega$ @ $V_{GS} = -10V$
  $R_{DS(ON)} = 0.12\Omega$ @ $V_{GS} = -4.5V$
- High density cell design for extremely low $R_{DS(ON)}$.
- Enhanced SuperSOT^{TM}-8 small outline surface mount package with high power and current handling capability.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	NDH8504P	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	±20	V
I_D	Drain Current - Continuous (Note 1)	-2.5	A
	- Pulsed	-7.5	
P_D	Maximum Power Dissipation (Note 1)	0.8	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	156	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2.5 A			0.08	Ω
		V_{GS} = -4.5 V, I_D = -2 A			0.12	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-7.5			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	-3			
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.67	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.67 A (Note 2)			-1.2	V

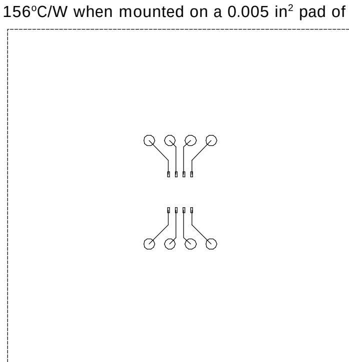
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

156°C/W when mounted on a 0.005 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.