National Semiconductor™

February 1997

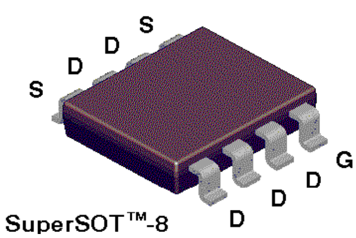
NDH833N
N-Channel Enhancement Mode Field Effect Transistor

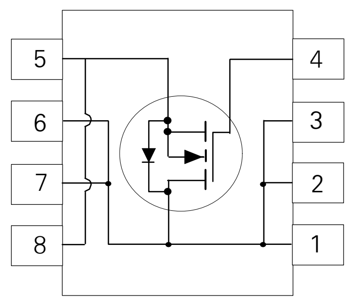
General Description

SuperSOT™-8 N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as battery powered circuits or portable electronics where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 7.1 A, 20 V. $R_{DS(ON)} = 0.020\ \Omega$ @ $V_{GS} = 4.5$ V
  $R_{DS(ON)} = 0.025\ \Omega$ @ $V_{GS} = 2.7$ V.
- Proprietary SuperSOT™-8 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.





Absolute Maximum Ratings T_A = 25°C unless otherwise note

Symbol	Parameter		NDH833N	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±8	V
I_D	Drain Current - Continuous	(Note 1a)	7.1	A
	- Pulsed		24	
P_D	Maximum Power Dissipation	(Note 1a)	1.8	W
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J= 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4	0.62	1	V
		T_J= 125°C	0.3	0.4	0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 7.1 A		0.015	0.02	Ω
		T_J= 125°C		0.022	0.036	
		V_{GS} = 2.7 V, I_D = 6.7 A		0.018	0.025	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	24			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7.1 A		35		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		1540		pF
C_{oss}	Output Capacitance			750		pF
C_{rss}	Reverse Transfer Capacitance			265		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 5 V, I_D = 1 A, V_{GEN} = 4.5 V, R_{GEN} = 6 Ω		12	20	ns
t_r	Turn - On Rise Time			35	70	ns
$t_{D(off)}$	Turn - Off Delay Time			110	200	ns
t_f	Turn - Off Fall Time			60	120	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 7.1 A, V_{GS} = 10 V		97	140	nC
Q_{gs}	Gate-Source Charge			8		nC
Q_{gd}	Gate-Drain Charge			33		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Units**
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)		0.65	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

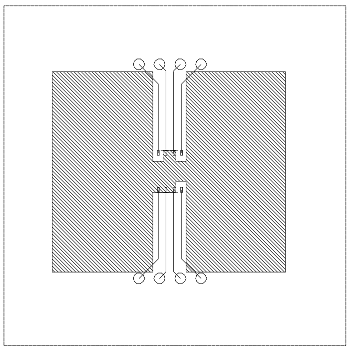
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

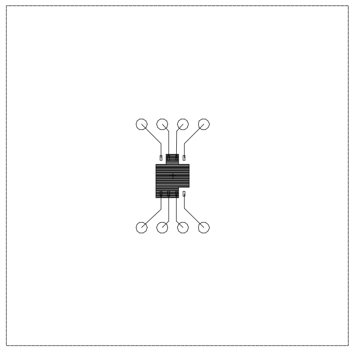
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

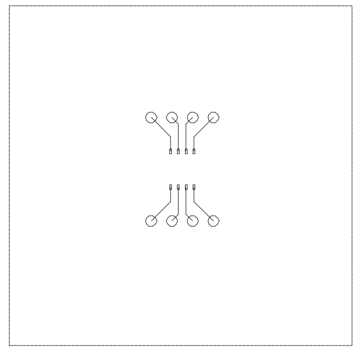
a. 70°C/W when mounted on a 1 in^2 pad of 2oz cpper.

b. 125°C/W when mounted on a 0.026 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.005 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

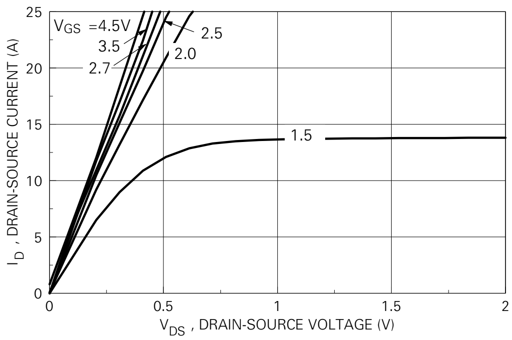


Figure 1. On-Region Characteristics.

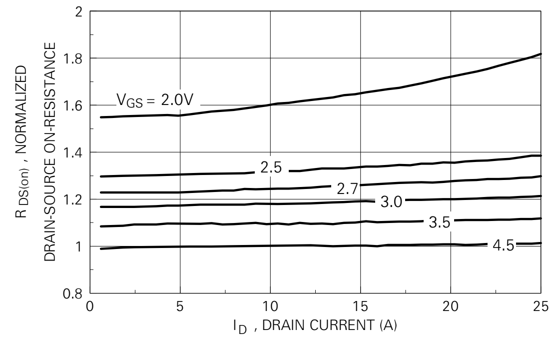


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

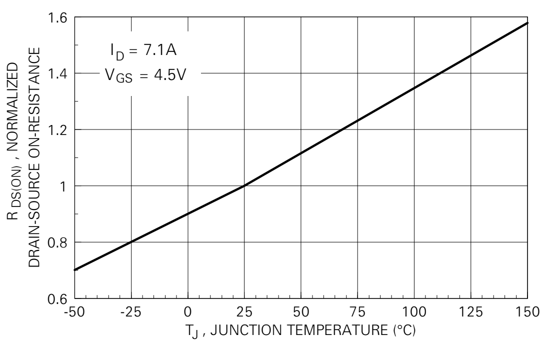


Figure 3. On-Resistance Variation with Temperature.

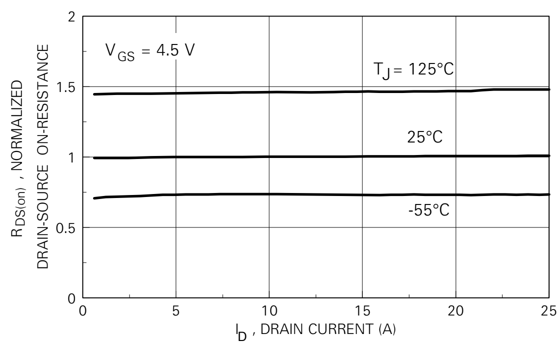


Figure 4. On-Resistance Variation with Drain Current and Temperature.

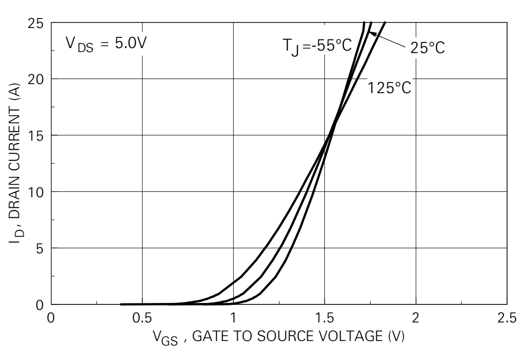


Figure 5. Transfer Characteristics.

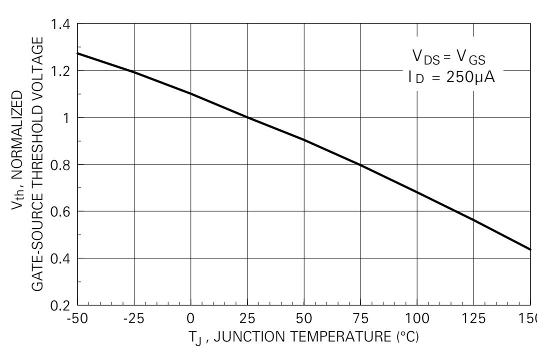


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

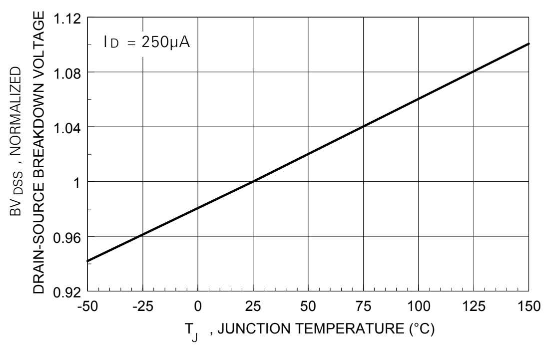


Figure 7. Breakdown Voltage Variation with Temperature.

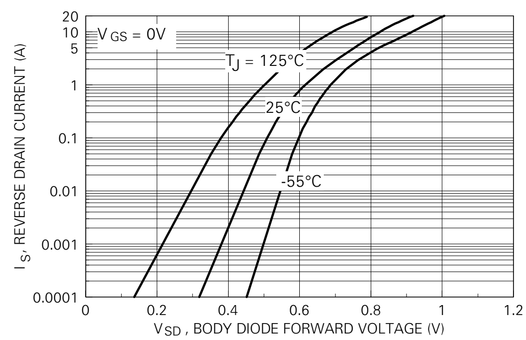


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

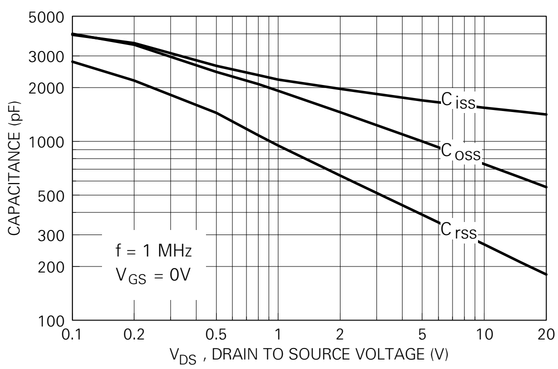


Figure 9. Capacitance Characteristics.

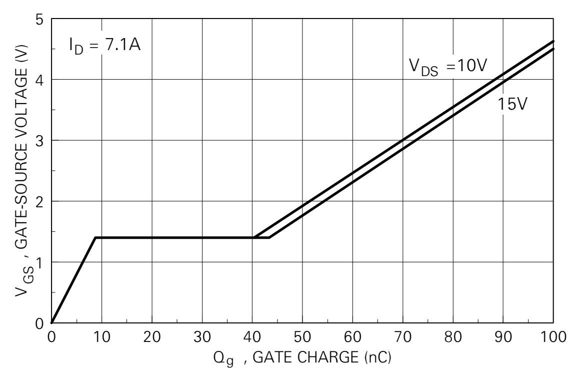


Figure 10. Gate Charge Characteristics.

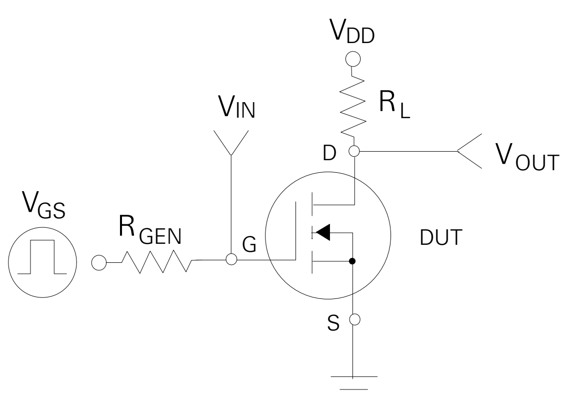


Figure 11. Switching Test Circuit.

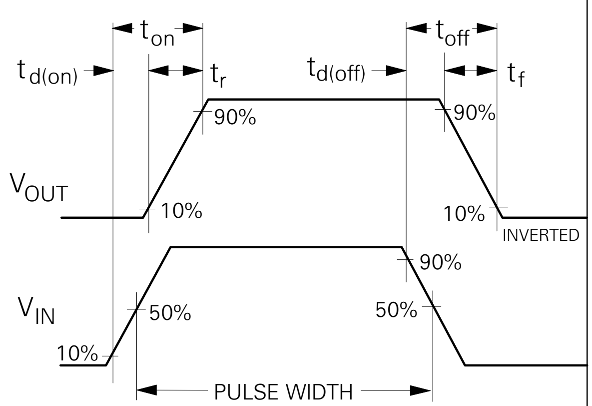


Figure 12. Switching Waveforms.

Typical Electrical and Thermal Characteristics (continued)

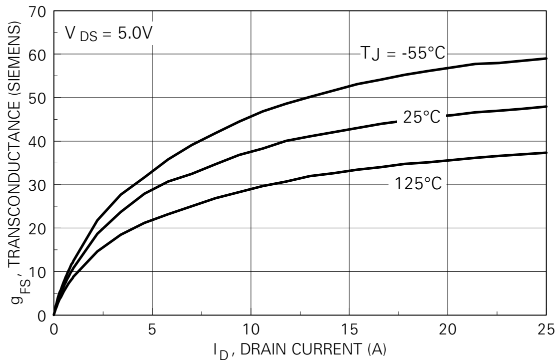


Figure 13. Transconductance Variation with Drain Current and Temperature.

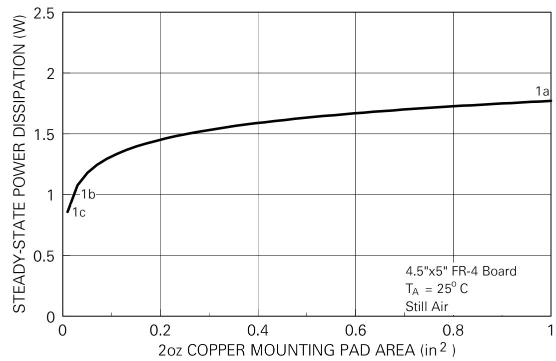


Figure 14. SuperSOT™-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

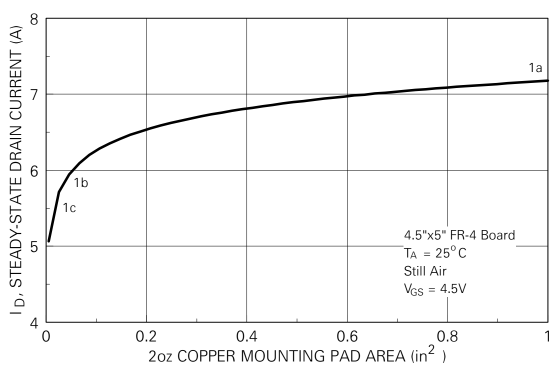


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

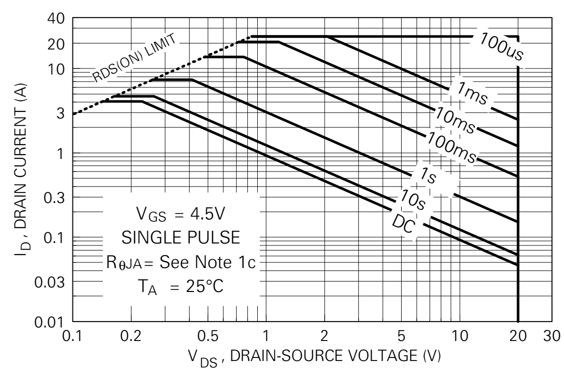


Figure 16. Maximum Safe Operating Area.

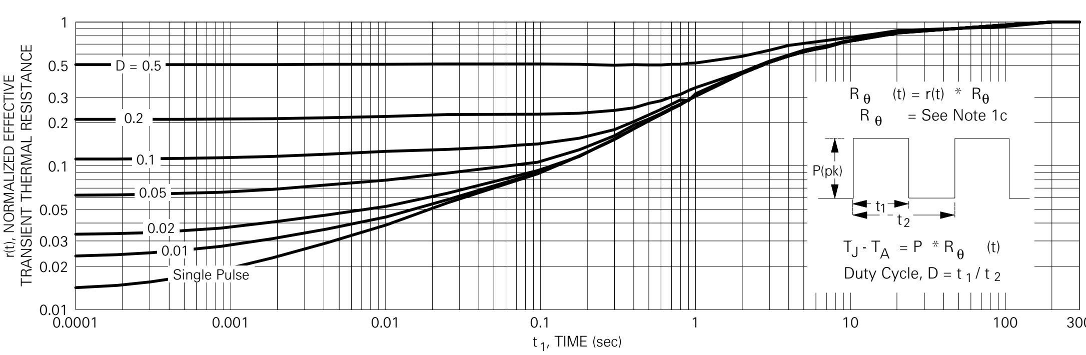


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.