

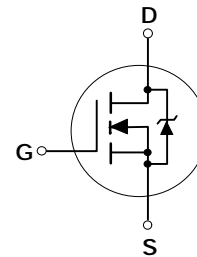
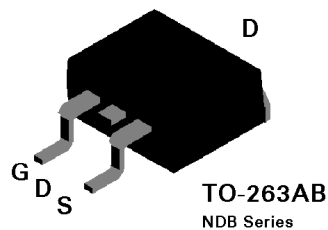
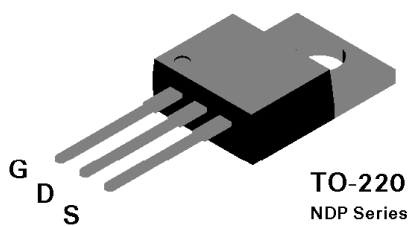
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NDP7061L / NDB7061L**N-Channel Logic Level Enhancement Mode Field Effect Transistor****General Description**

These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 60 A, 60 V. $R_{DS(ON)} = 0.018 \Omega @ V_{GS} = 5 \text{ V}$
 $R_{DS(ON)} = 0.013 \Omega @ V_{GS} = 10 \text{ V}$.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)} < 2.0\text{V}$.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D²PAK) package for both through hole and surface mount applications.

**Absolute Maximum Ratings** $T_c = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDP7061L	NDB7061L	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1 \text{ M}\Omega$)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
	- Nonrepetitive ($t_p < 50 \mu\text{s}$)	± 25		
I_D	Drain Current - Continuous	60		A
	- Pulsed	180		
P_D	Maximum Power Dissipation @ $T_c = 25^\circ\text{C}$	130		W
	Derate above 25°C	0.87		
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		$^\circ\text{C}$

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	V _{DD} = 30 V, I _D = 60 A			500	mJ
I _{AR}	Maximum Drain-Source Avalanche Current				60	A
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V			10	μA
		T _J = 125°C			1	mA
I _{GSSF}	Gate - Body Leakage, Forward	V _{GS} = 16 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate - Body Leakage, Reverse	V _{GS} = -16 V, V _{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	1.2	2	V
		T _J = 125°C	0.65	0.7	1.5	
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 5 V, I _D = 30 A		0.013	0.018	Ω
		T _J = 125°C		0.023	0.032	
		V _{GS} = 10 V, I _D = 30 A		0.011	0.013	
I _{D(on)}	On-State Drain Current	V _{GS} = 5 V, V _{DS} = 10 V	60			A
g _{FS}	Forward Transconductance	V _{DS} = 10 V, I _D = 30 A		45		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{DS} = 30 V, V _{GS} = 0 V, f = 1.0 MHz		2600		pF
C _{OSS}	Output Capacitance			690		pF
C _{RSS}	Reverse Transfer Capacitance			220		pF
SWITCHING CHARACTERISTICS (Note 1)						
t _{D(on)}	Turn - On Delay Time	V _{DD} = 30 V, I _D = 60A,		18	35	nS
t _r	Turn - On Rise Time	V _{GS} = 5 V, R _{GEN} = 10 Ω		430	600	nS
t _{D(off)}	Turn - Off Delay Time	R _{GS} = 10 Ω		63	120	nS
t _f	Turn - Off Fall Time			240	400	nS
Q _g	Total Gate Charge	V _{DS} = 12 V		52	75	nC
Q _{gs}	Gate-Source Charge	I _D = 60 A, V _{GS} = 5 V		9		nC
Q _{gd}	Gate-Drain Charge			28		nC

Electrical Characteristics ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				60	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				180	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}$ (Note 1)		0.9	1.3	V
			$T_J = 125^\circ\text{C}$	0.8	1.2	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_F = 60\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$	40		150	ns
I_{rr}	Reverse Recovery Current		2		10	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.15	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	$^\circ\text{C}/\text{W}$

Note:

1. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

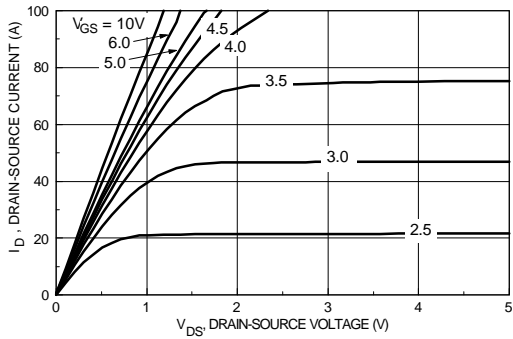


Figure 1. On-Region Characteristics.

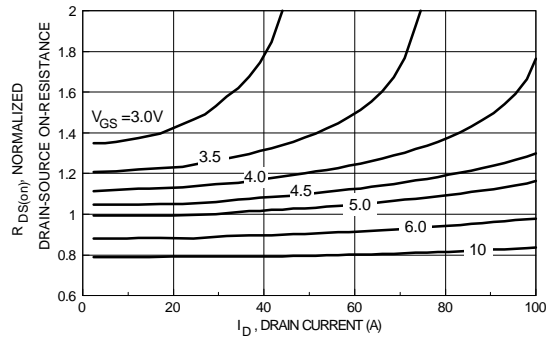


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

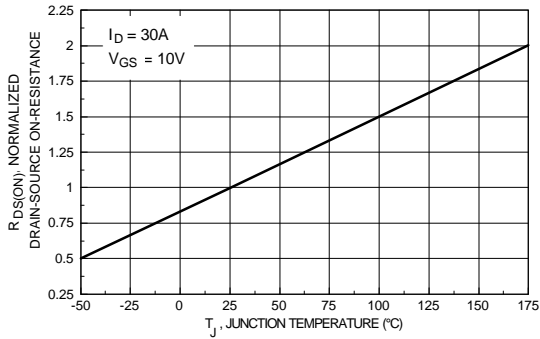


Figure 3. On-Resistance Variation with Temperature.

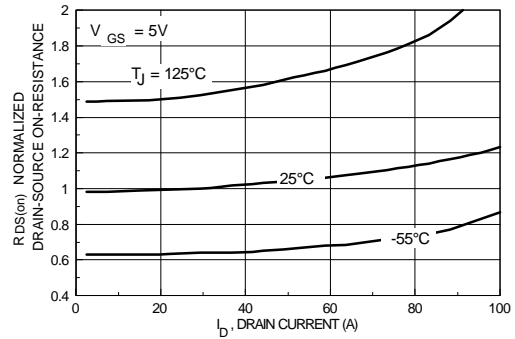


Figure 4. On-Resistance Variation with Drain Current and Temperature.

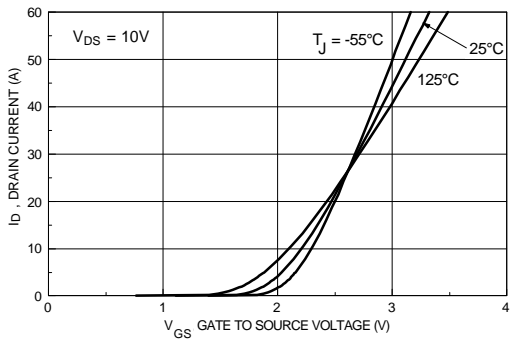


Figure 5. Transfer Characteristics.

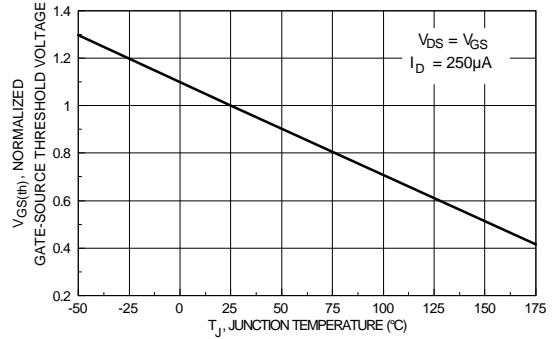


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

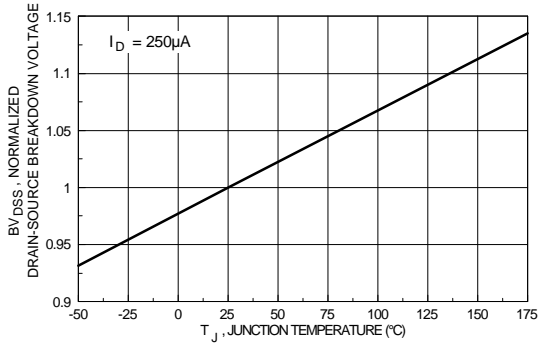


Figure 7. Breakdown Voltage Variation with Temperature.

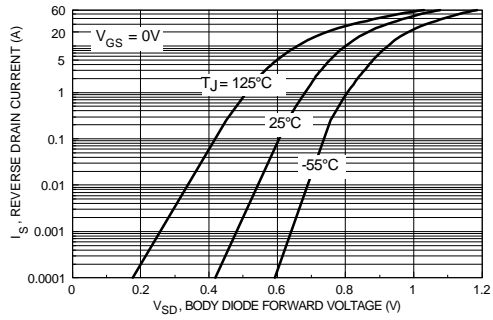


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

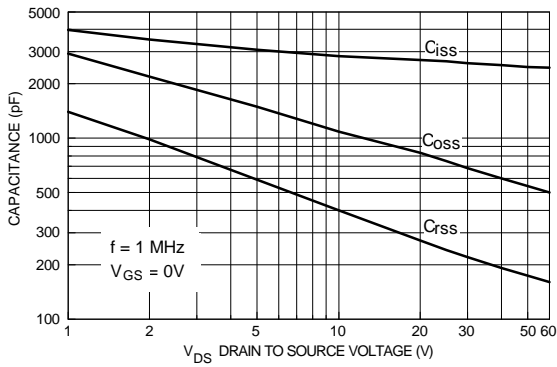


Figure 9. Capacitance Characteristics.

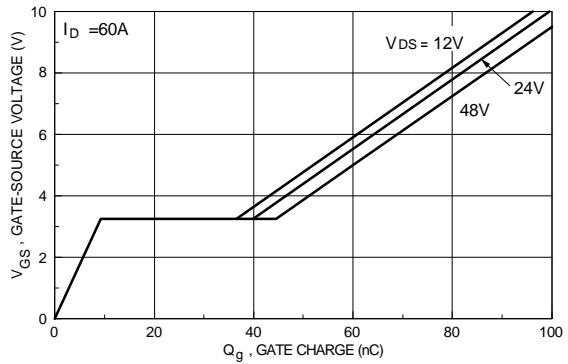


Figure 10. Gate Charge Characteristics.

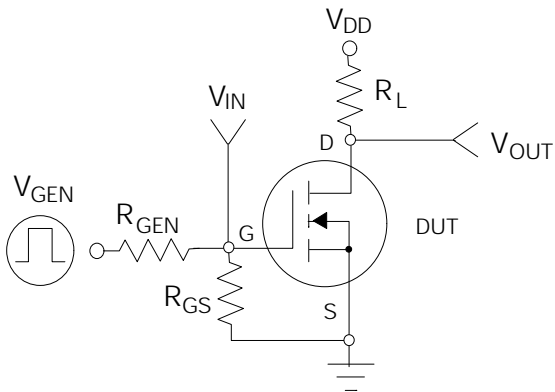


Figure 11. Switching Test Circuit.

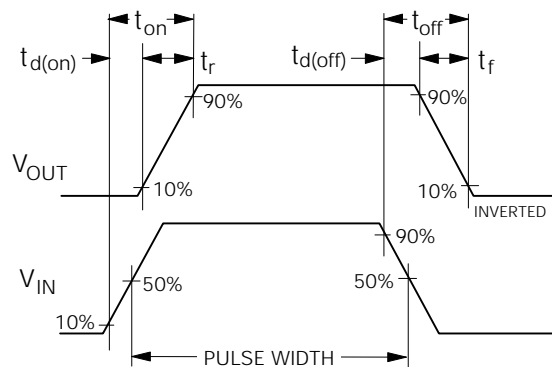


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

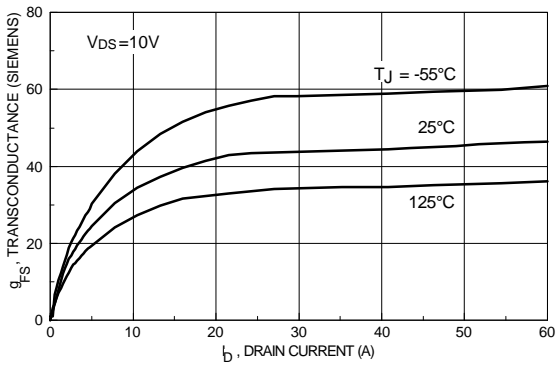


Figure 13. Transconductance Variation with Drain Current and Temperature.

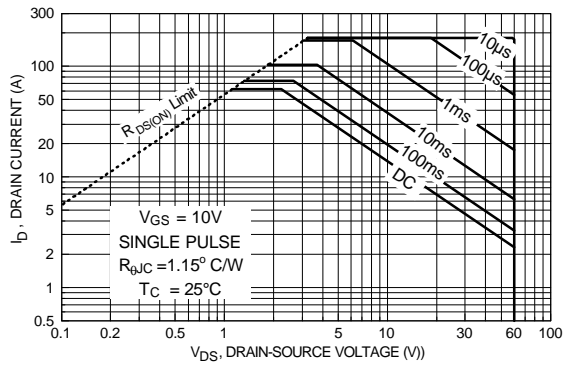


Figure 14. Maximum Safe Operating Area.

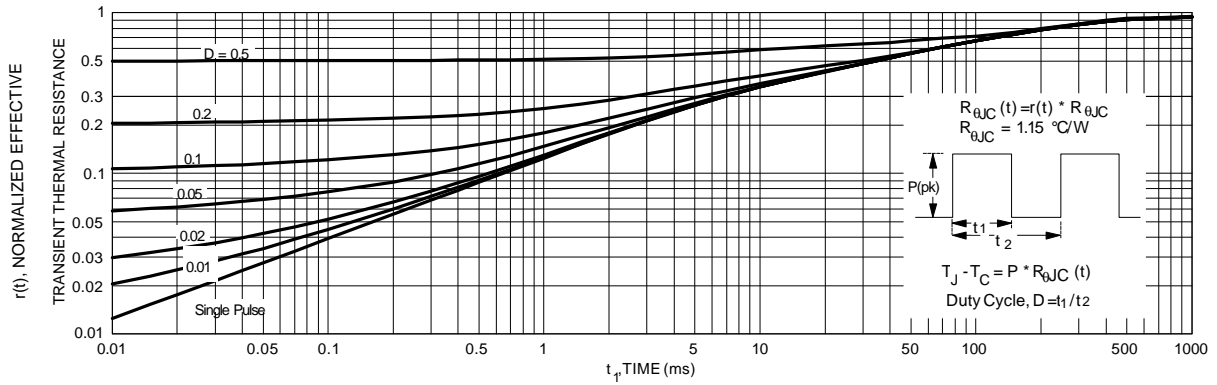


Figure 15. Transient Thermal Response Curve.