RFP25N06, RF1S25N06, RF1S25N06SM

25A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- **25A, 60V**
- **$r_{DS(ON)}$ = 0.047Ω**
- ***Temperature Compensating* PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**
- **+175°C Operating Temperature**

Description

The RFP25N06, RF1S25N06, and RF1S25N06SM N-Channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

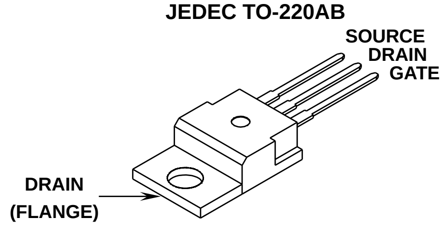
PART NUMBER	PACKAGE	BRAND
RFP25N06	TO-220AB	RFP25N06
RF1S25N06	TO-262AA	F1S25N06
RF1S25N06SM	TO-263AB	F1S25N06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S25N06SM9A.

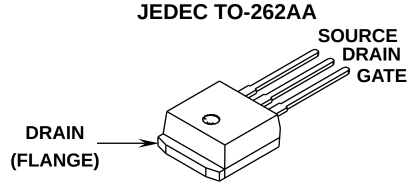
Formerly developmental type TA09771.

Packages

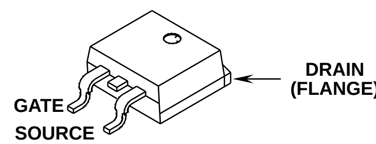
JEDEC TO-220AB



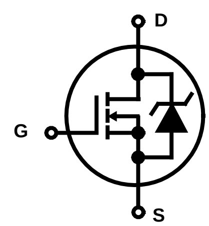
JEDEC TO-262AA



JEDEC TO-263AB



Symbol



Absolute Maximum Ratings T_C = +25°C, Unless Otherwise Specified

		RFP25N06, RF1S25N06, RF1S25N06SM	UNITS
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGR}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	25	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
T_C = +25°C	P_D	72	W
Derate above +25°C		0.48	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **1492.3**

Electrical Specifications
T_C = +25^{o}C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25^{o}C	-	-	1	μA
			T_C = +150^{o}C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 25A, V_{GS} = 10V		-	-	0.047	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 12.5A, R_L = 2.4Ω, V_{GS} = 10V, R_{GS} = 10Ω		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	14	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	45	-	ns
Fall Time	t_F			-	22	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 48V, I_D = 25A, R_L = 1.92Ω	-	-	80	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0V to 10V		-	-	45	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 2V		-	-	3	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	975	-	pF
Output Capacitance	C_{OSS}			-	330	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	95	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	2.083	^{o}C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$			-	-	80	^{o}C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 25A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 25A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves

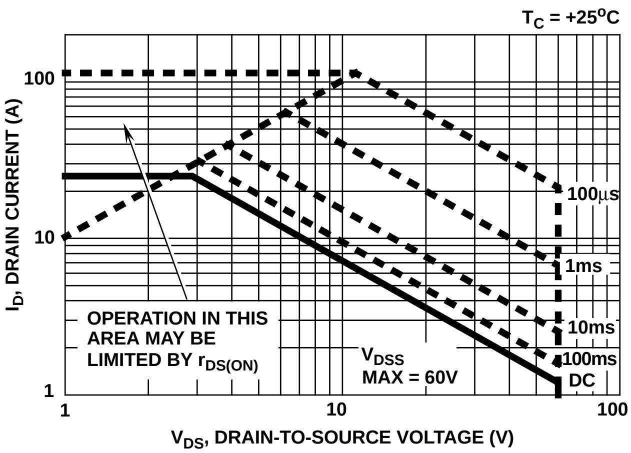


FIGURE 1. SAFE OPERATING AREA CURVE

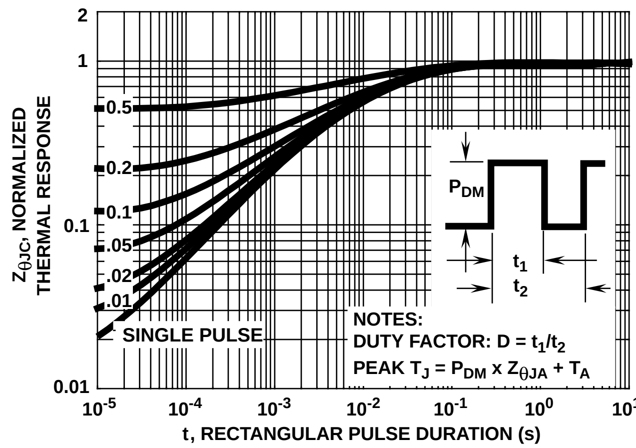


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

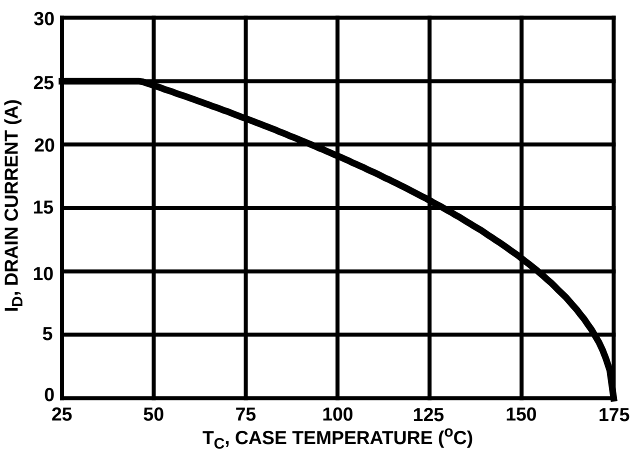


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

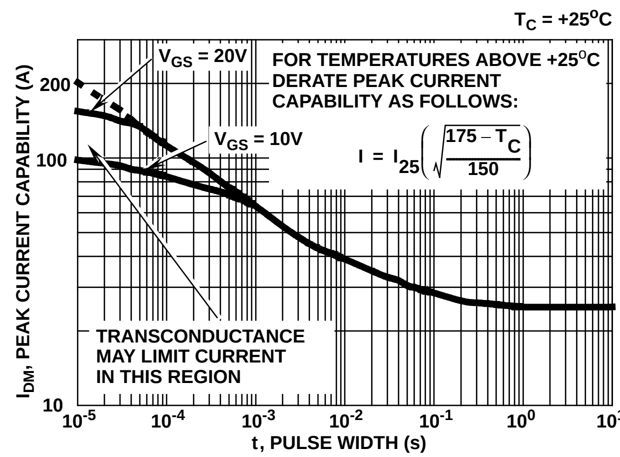


FIGURE 4. PEAK CURRENT CAPABILITY

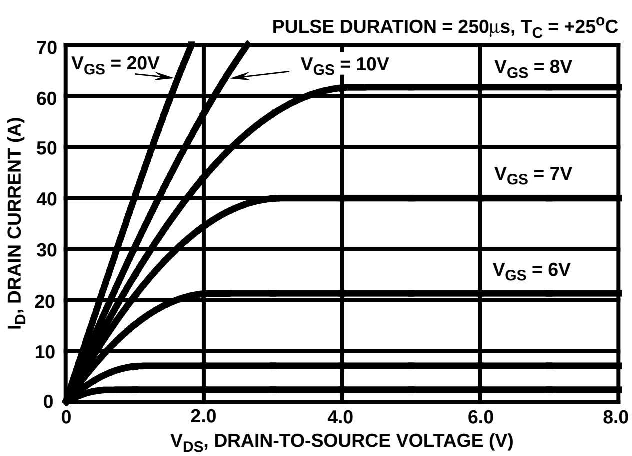


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

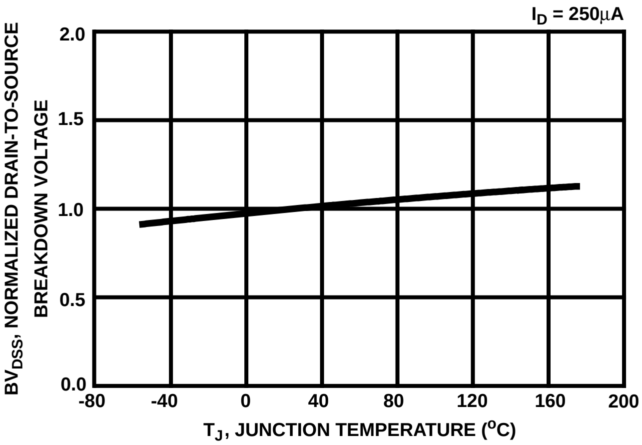


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

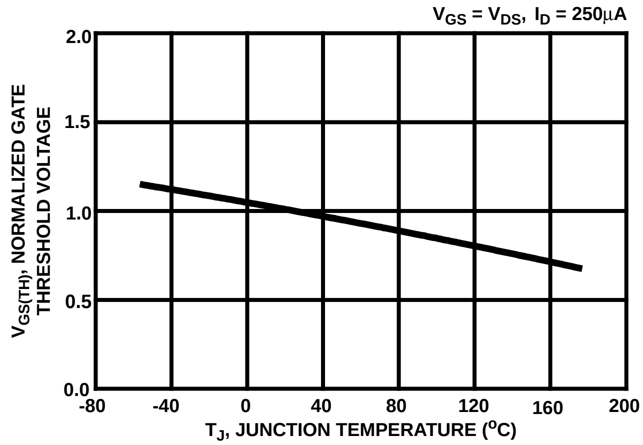


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

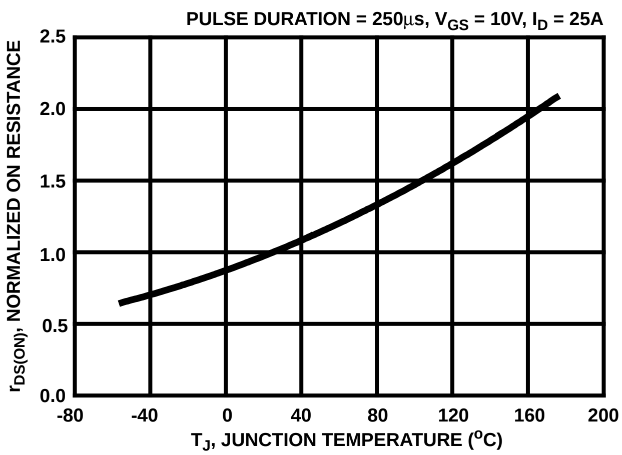


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

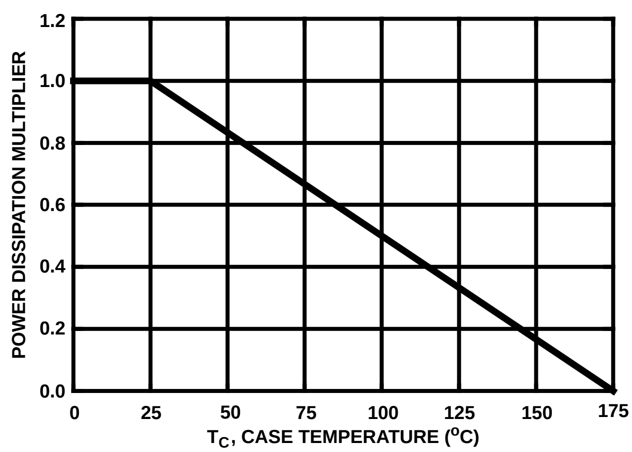


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

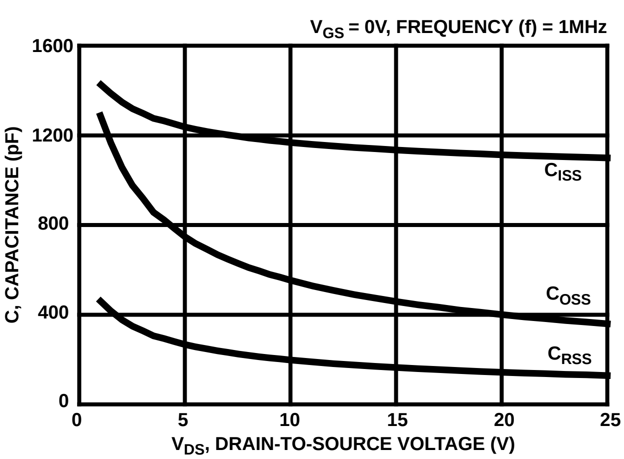


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

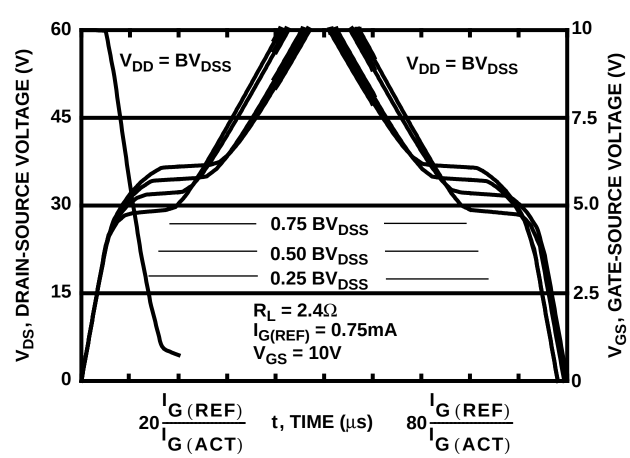


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

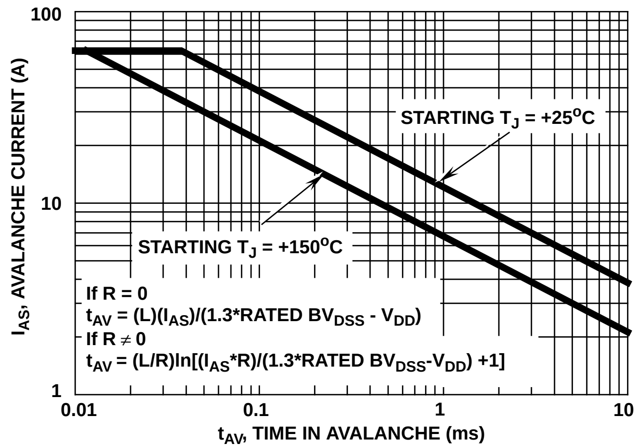


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING.

REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

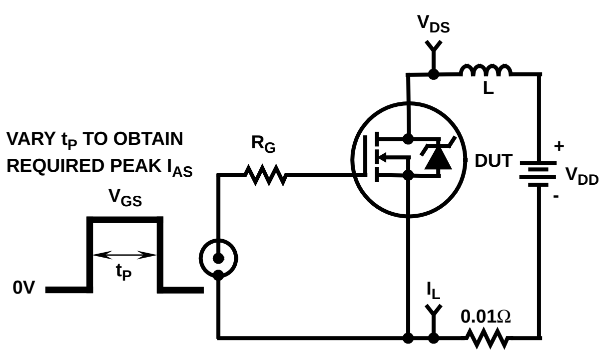


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

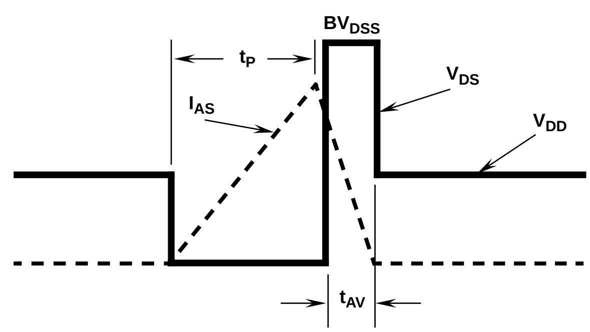


FIGURE 15. UNCLAMPED ENERGY WAVEFORM

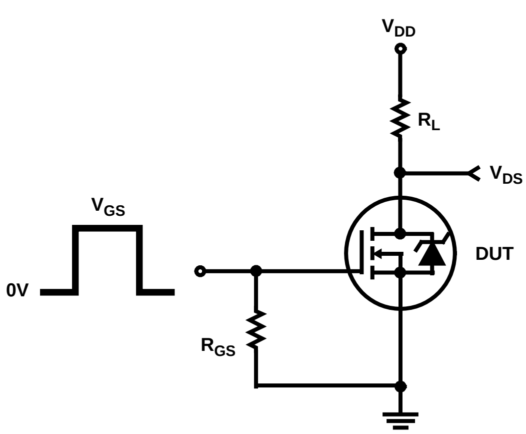


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

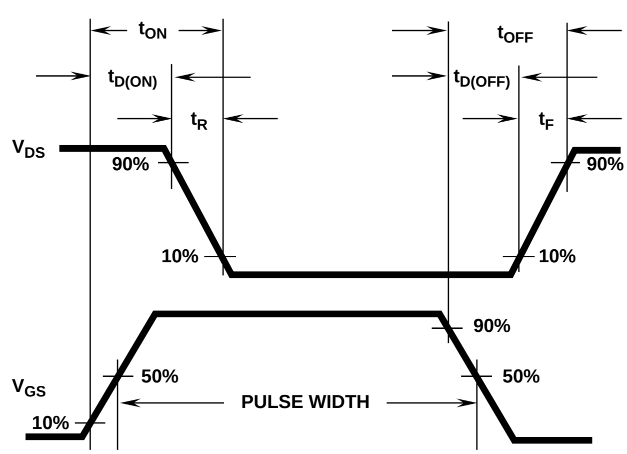
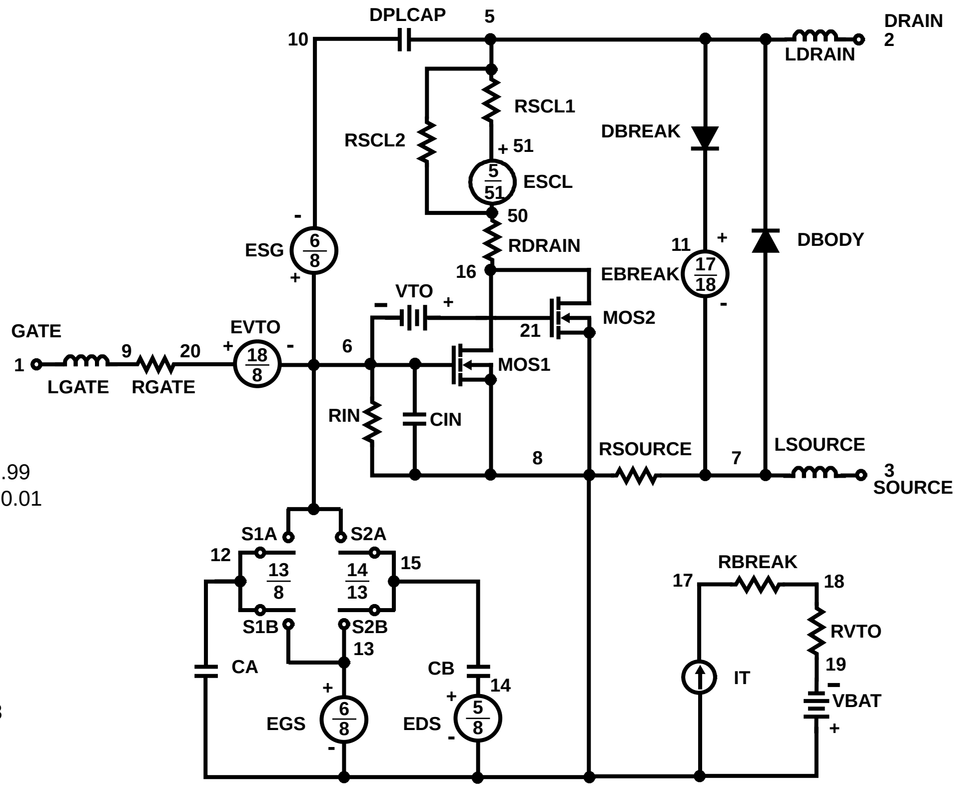


FIGURE 17. RESISTIVE SWITCHING WAVEFORM

Temperature Compensated PSPICE Model for the RFP25N06, RF1S25N06, RF1S25N06SM

```
.SUBCKT    RFP25N06  2 1 3 ;        rev 8/19/94

CA  12  8  1.83e-9
CB  15  14  1.98e-9
CIN  6  8  9.7e-10

DBODY  7  5  DBDMOD
DBREAK  5 11  DBKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18  65.9
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTO  20  6  18  8  1

IT  8  17  1

LDRAIN  2  5  1e-9
LGATE 1  9  4.92e-9
LSOURCE  3  7  4.5e-9

MOS1  16  6  8  8  MOSMOD  M = 0.99
MOS2  16  21  8  8  MOSMOD  M = 0.01

RBREAK  17  18  RBKMOD  1
RDRAIN  50  16  RDSMOD  1.1e-3
RGATE  9  20  2.88
RIN  6  8  1e9
RSCL1  5  51  RSCLMOD 1e-6
RSCL2  5  50  1e3
RSOURCE  8  7  RDSMOD  20.3e-3
RVTO  18  19  RVTOMOD  1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT  8  19  DC  1
VTO  21  6   0.764

ESCL  51 50  VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/108,6))}

.MODEL DBDMOD D (IS = 2.32e-13  RS = 5.72e-3  TRS1 = 2.56e-3  TRS2 = -5.13e-6  CJO = 1.18e-9  TT = 5.62e-8)
.MODEL DBKMOD D (RS = 2.00e-1  TRS1 = 3.33e-4  TRS2 = 2.68e-6)
.MODEL DPLCAPMOD D (CJO = 6.55e-10  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 3.89  KP = 15.03  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 1.04e-3  TC2 = -1.04e-6)
.MODEL RDSMOD RES (TC1 = 5.85e-3  TC2 = 1.77e-5)
.MODEL RSCLMOD RES (TC1 = 2.0e-3  TC2 = 1.5e-6)
.MODEL RVTOMOD RES (TC1 = -5.35e-3  TC2 = -3.77e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -5.04  VOFF= -3.04)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.04  VOFF= -5.04)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.02  VOFF= 1.98)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 1.98  VOFF= -3.02)

.ENDS
```



NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.