IRF140, IRF141, IRF142, IRF143

28A and 25A, 80V and 100V, 0.077 and 0.100 Ohm, N-Channel Power MOSFETs

July 1998

Features

- **28A and 25A, 80V and 100V**
- **$r_{DS(ON)}$ = 0.077Ω and 0.100Ω**
- **Single Pulse Avalanche Energy Rated**
- **SOA is Power-Dissipation Limited**
- **Nanosecond Switching Speeds**
- **Linear Transfer Characteristics**
- **High Input Impedance**
- **Majority Carrier Device**

Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

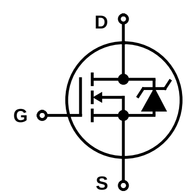
Formerly developmental type TA17421.

Ordering Information

PART NUMBER	PACKAGE	BRAND
IRF140	TO-204AE	IRF140
IRF141	TO-204AE	IRF141
IRF142	TO-204AE	IRF142
IRF143	TO-204AE	IRF143

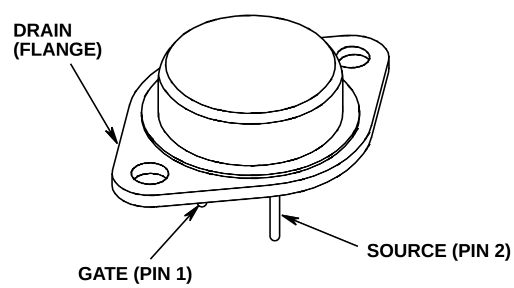
NOTE: When ordering, use the entire part number.

Symbol



Packaging

JEDEC TO-204AE



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

	IRF140	IRF141	IRF142	IRF143	UNITS
Drain to Source Voltage (Note 1) . . . . V_{DS}	100	80	100	80	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1) . . . . V_{DGR}	100	80	100	80	V
Continuous Drain Current. . . . . I_D	28	28	25	25	A
$T_C = 100^oC$. . . . . I_D	20	20	17	17	A
Pulsed Drain Current (Note 3) . . . . I_{DM}	110	110	100	100	A
Gate To Source Voltage . . . . V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation . . . . P_D	150	150	150	150	W
Linear Derating Factor	1.0	1.0	1.0	1.0	W/^{o}C
Single Pulse Avalanche Energy Rating (Note 4) . . . . E_{AS}	100	100	100	100	mJ
Operating and Storage Temperature . . . . T_J, T_{STG}	-55 to 175	-55 to 175	-55 to 175	-55 to 175	^{o}C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s . . . . T_L	300	300	300	300	^{o}C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

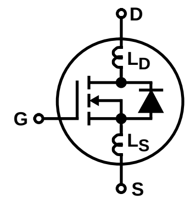
NOTE:

1. $T_J = 25^oC$ to 150^oC.

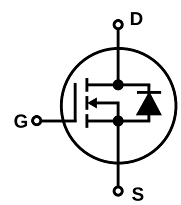
Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 10)				
IRF140, IRF142			100	-	-	V
IRF141, IRF143			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, I_D = 250μA	2.0	-	4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_J = 150^oC$	-	-	250	μA
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, V_{GS} = 10V				
IRF140, IRF141			28	-	-	A
IRF142, IRF143			25	-	-	A
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V	-	-	±100	nA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 17A, V_{GS} = 10V (Figure 8, 9)				
IRF140, IRF141			-	0.07	0.077	Ω
IRF142, IRF143			-	0.09	0.100	Ω
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, I_D = 17A (Figure 12)	8.7	13	-	S
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 50V, I_D ≈ 28A, R_G = 9.1Ω, R_L = 1.7Ω (Figures 17, 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	16	23	ns
Rise Time	t_r		-	27	110	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	38	60	ns
Fall Time	t_f		-	14	75	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 10V, I_D = 28A, V_{DS} = 0.8 x Rated BV_{DSS} $I_{g(REF)}$ = 1.5mA (Figures 14, 19, 20) Gate Charge is Essentially Independent of Operating Temperature	-	38	59	nC
Gate to Source Charge	Q_{gs}		-	9	-	nC
Gate to Drain “Miller” Charge	Q_{gd}		-	21	-	nC

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz (Figure 11)	-	1275	-	pF
Output Capacitance	C_{OSS}		-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	160	-	pF
Internal Drain Inductance	L_D	Measured Between the Contact Screw on the Flange that is Closer to Source and Gate Pins and the Center of Die; Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Lead, 6mm (0.25in) From the Flange and the Source Bonding Pad	-	12.5	-	nH
Thermal Resistance, Junction to Case	$R_{\theta JC}$		-	-	1.0	$^oC/W$
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^oC/W$

SourceTo Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier. 	-	-	28	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	110	A
Drain to Source Diode Voltage (Note 2)	V_{SD}	$T_J = 25^oC$, $I_{SD} = 28A$, $V_{GS} = 0V$ (Figure 13)	-	-	2.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^oC$, $I_{SD} = 28A$, $dI_{SD}/dt = 100A/\mu s$	70	150	300	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 25^oC$, $I_{SD} = 28A$, $dI_{SD}/dt = 100A/\mu s$	0.44	0.9	1.9	μC

NOTES:

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 3).
4. $V_{DD} = 25V$, starting $T_J = 25^oC$, L = 190μH, $R_G = 25\Omega$, peak $I_{AS} = 28A$ (Figures 15, 16).

Typical Performance Curves

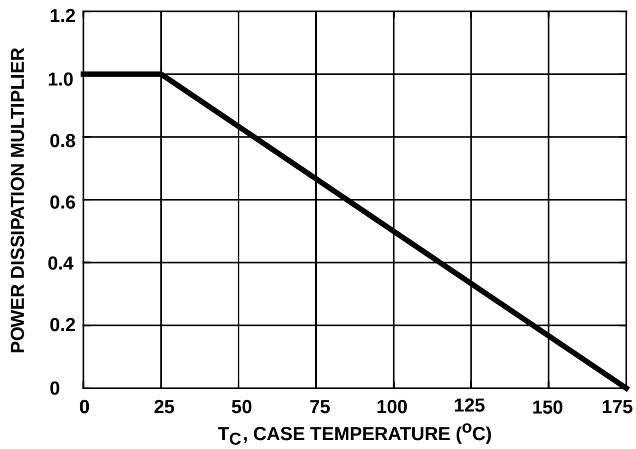


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

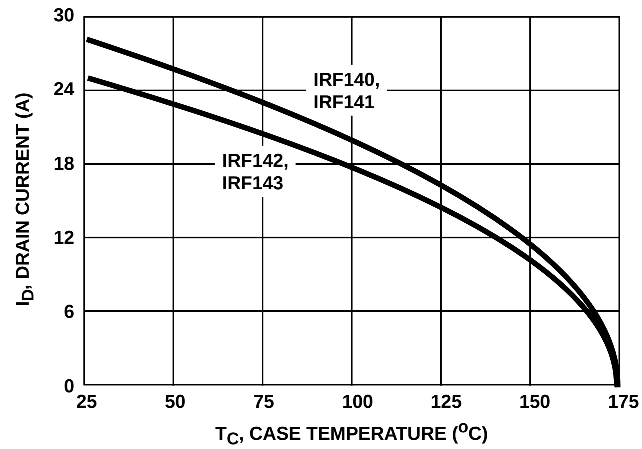


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

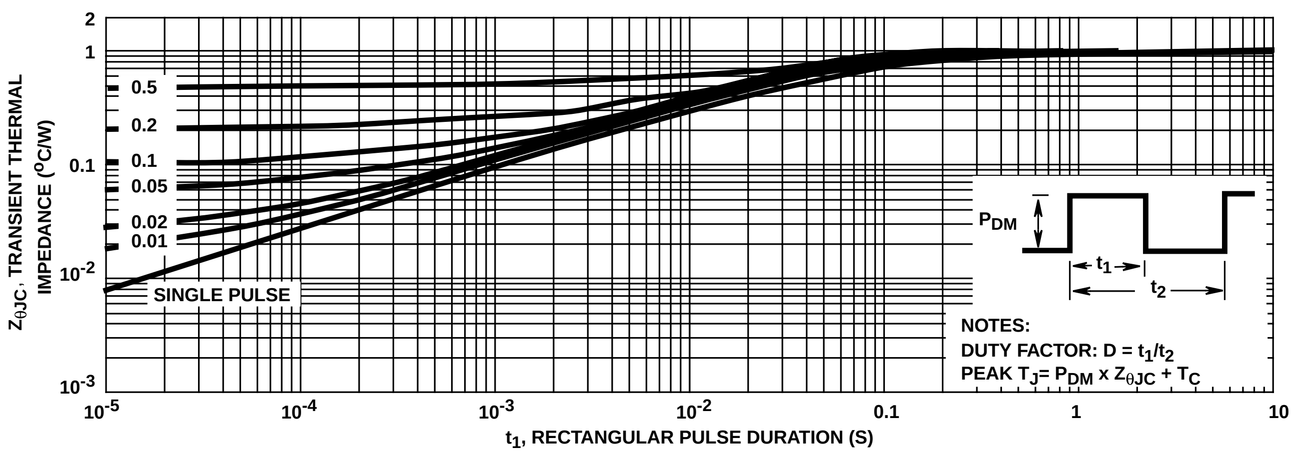


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

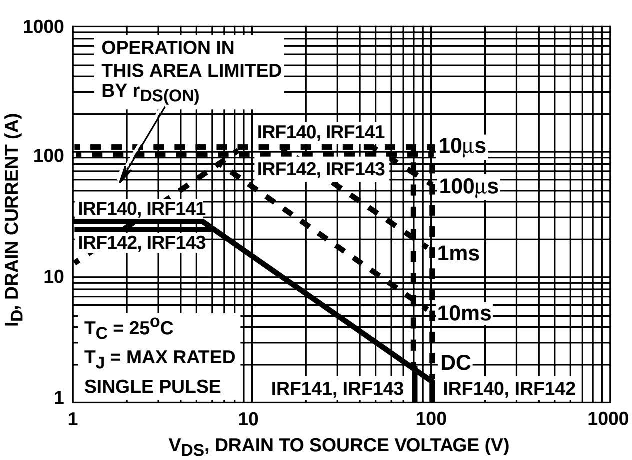


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

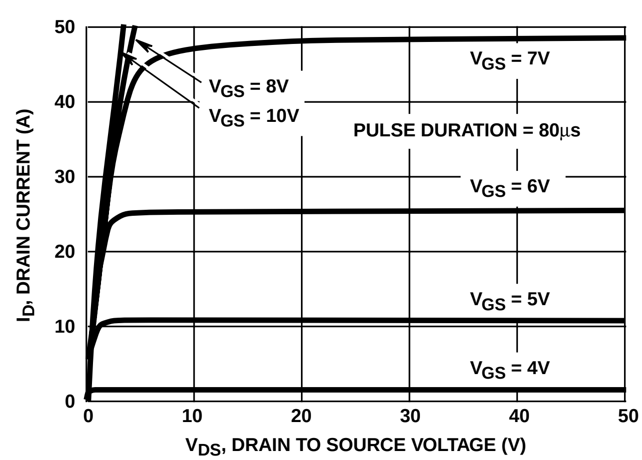


FIGURE 5. OUTPUT CHARACTERISTICS

Typical Performance Curves (Continued)

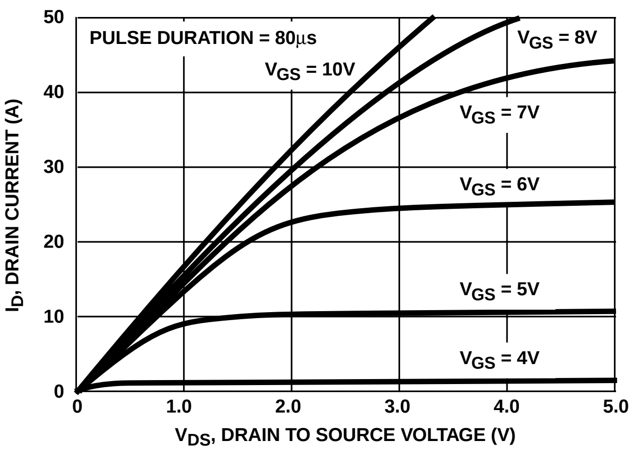


FIGURE 6. SATURATION CHARACTERISTICS

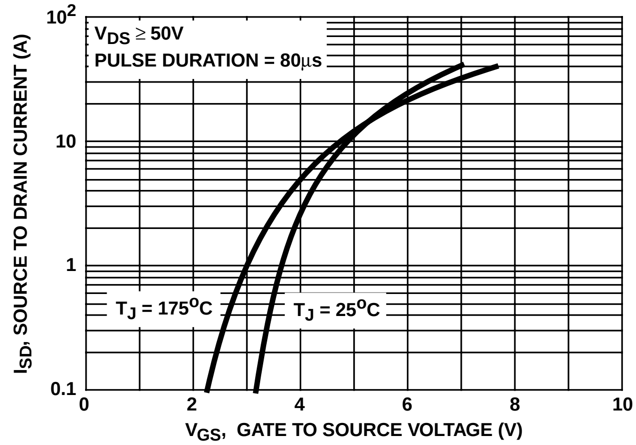


FIGURE 7. TRANSFER CHARACTERISTICS

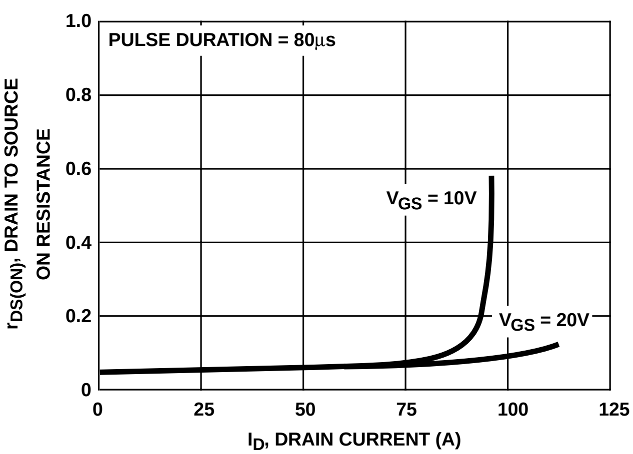


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

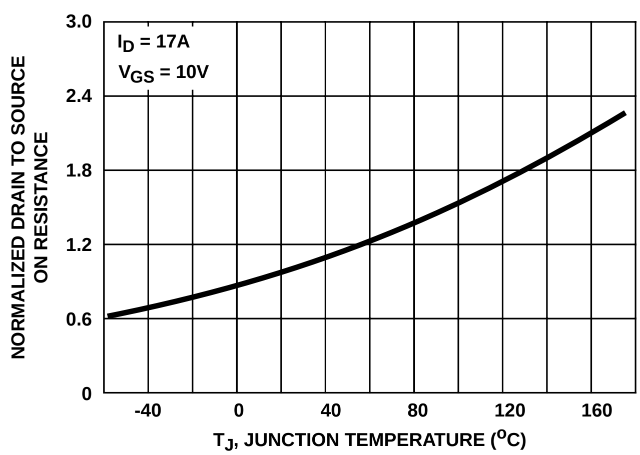


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

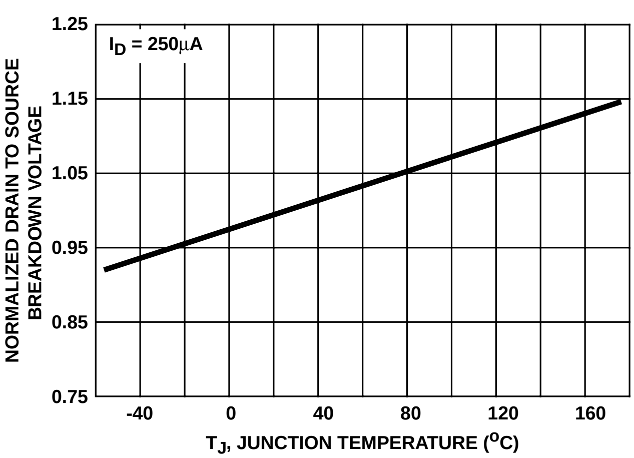


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

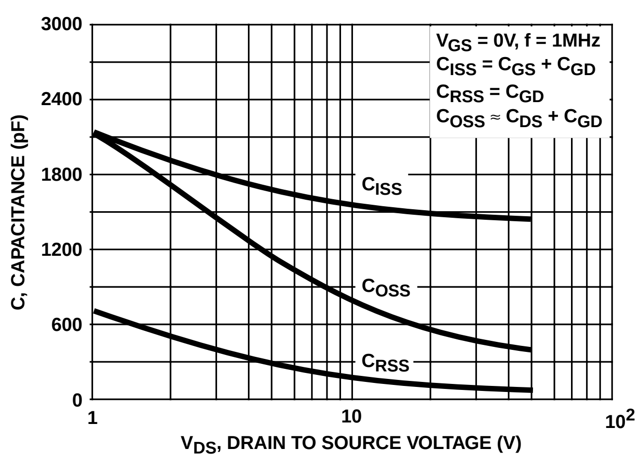


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

Typical Performance Curves (Continued)

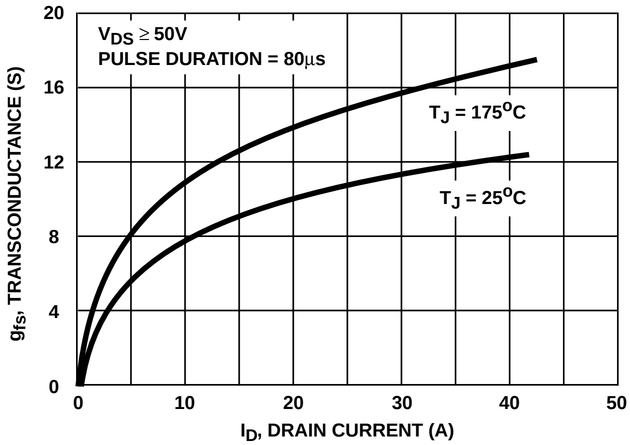


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

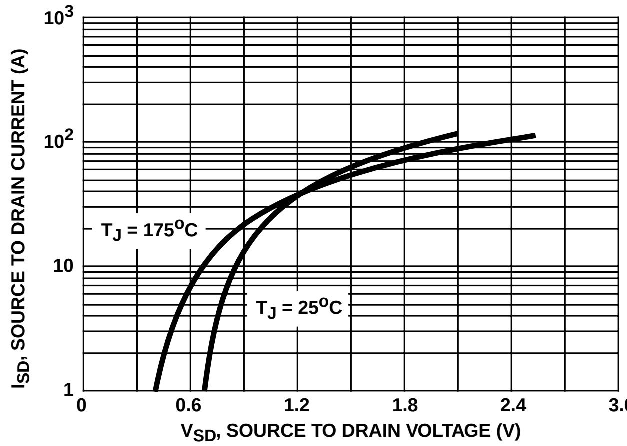


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

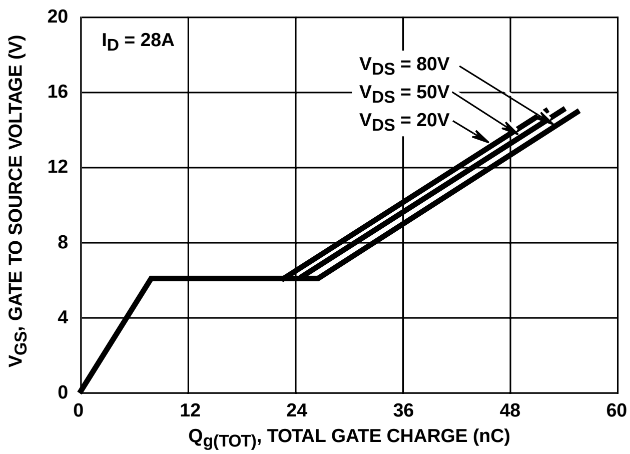


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

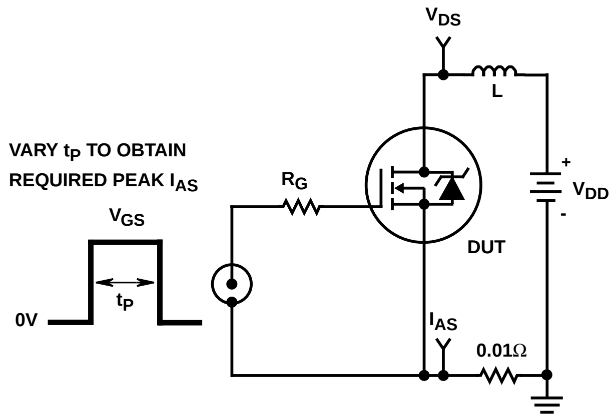


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

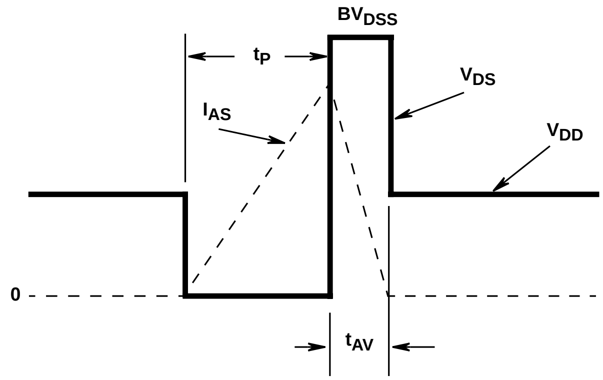


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

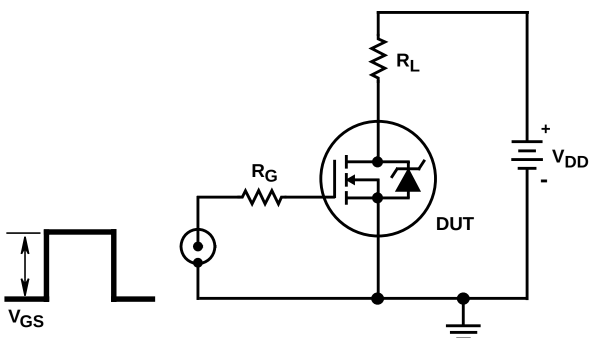


FIGURE 17. SWITCHING TIME TEST CIRCUIT

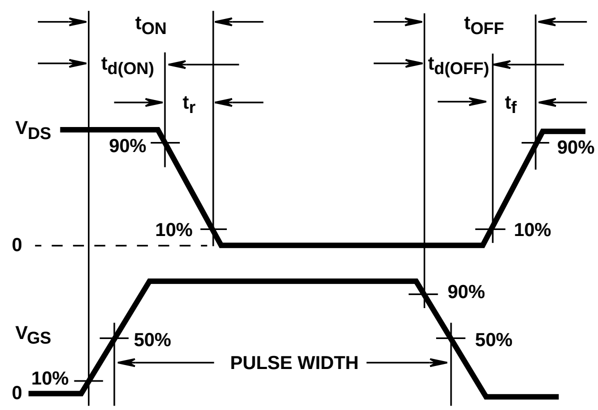


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

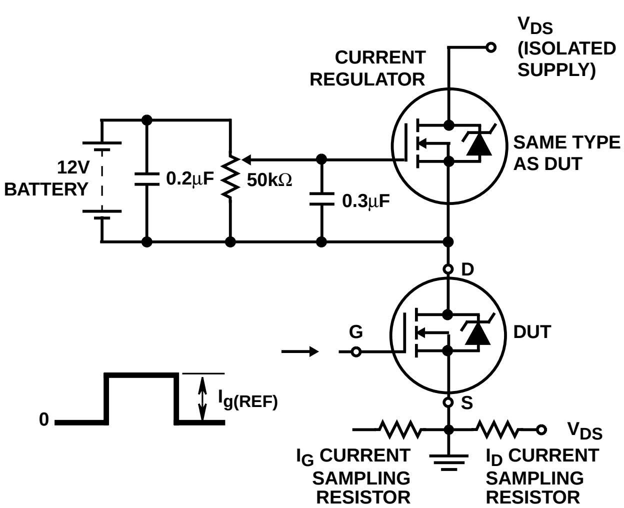


FIGURE 19. GATE CHARGE TEST CIRCUIT

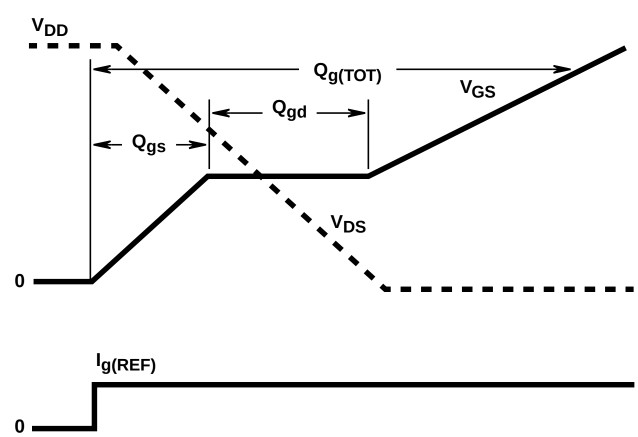


FIGURE 20. GATE CHARGE WAVEFORMS