

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# HAT3021R

Silicon N/P Channel Power MOS FET  
Power Switching

REJ03G0415-0200

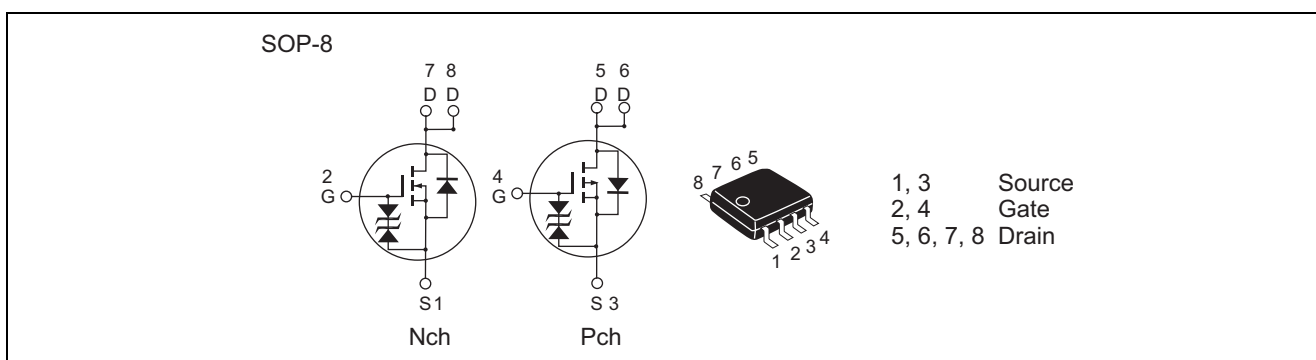
Rev.2.00

Oct.06.2004

## Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting

## Outline



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	$V_{DSS}$	80	-80	V
Gate to source voltage	$V_{GSS}$	±20	±20	V
Drain current	$I_D$	3.4	-2.6	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	20.4	-15.6	A
Body-drain diode reverse drain current	$I_{DR}$	3.4	-2.6	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	1.5	1.5	W
Channel temperature	$T_{ch}$	150		°C
Storage temperature	$T_{stg}$	-55 to +150		°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm),  $PW \leq 10s$

## Electrical Characteristics

(Ta = 25°C)

## • N Channel

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	80	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 80 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	90	115	$\text{m}\Omega$	$I_D = 1.7 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	100	145	$\text{m}\Omega$	$I_D = 1.7 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	4.2	7.0	—	S	$I_D = 1.7 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	400	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	57	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	24	—	pF	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	7.3	—	nC	$V_{DD} = 25 \text{ V}$
Gate to source charge	$Q_{gs}$	—	1.1	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	1.3	—	nC	$I_D = 3.4 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	6.0	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 1.7 \text{ A}$
Rise time	$t_r$	—	4.0	—	ns	$V_{DD} \cong 30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	39	—	ns	$R_L = 17.6 \text{ }\Omega$
Fall time	$t_f$	—	3.5	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.83	1.08	V	$I_F = 3.4 \text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	30	—	ns	$I_F = 3.4 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

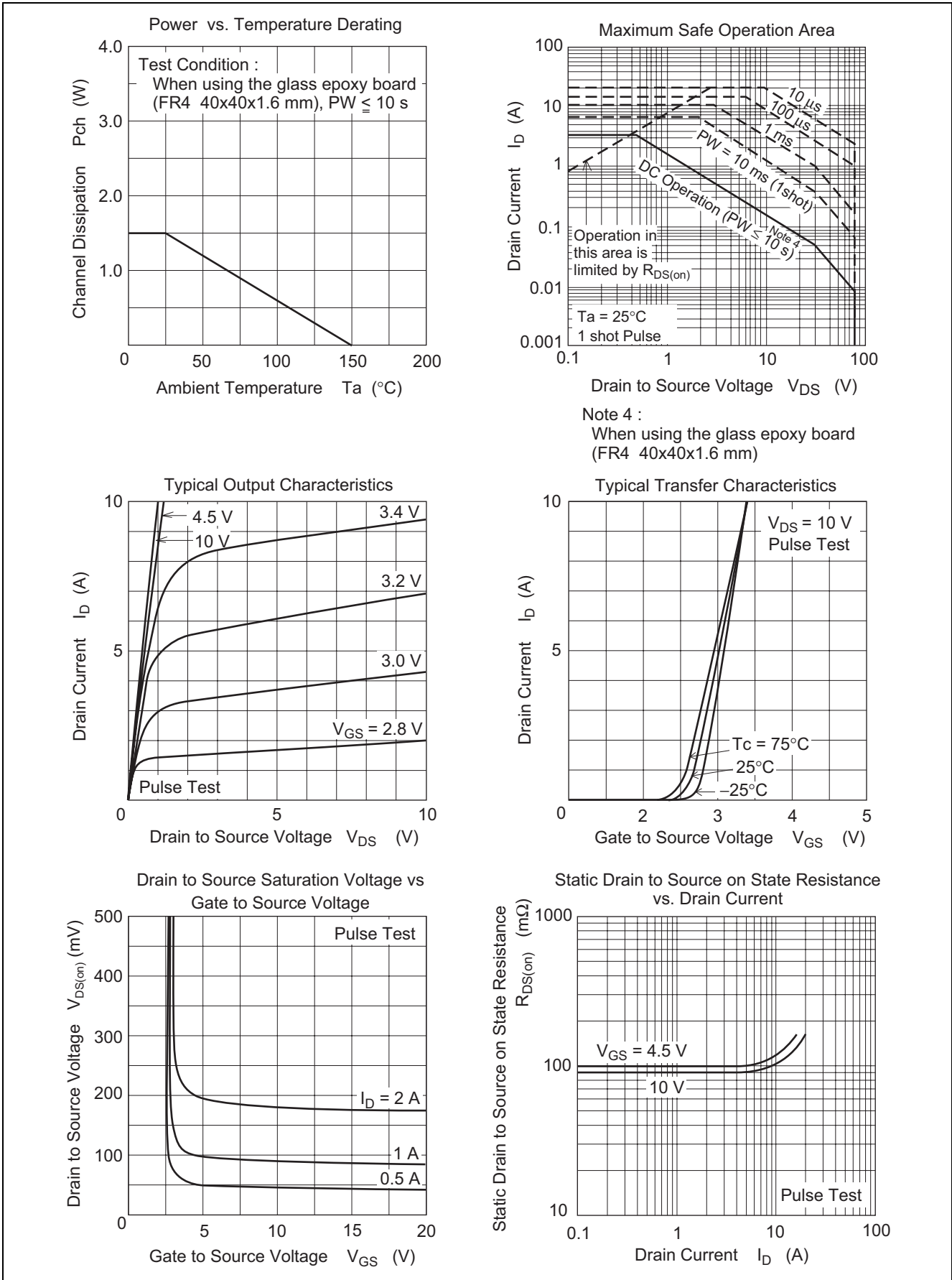
## • P Channel

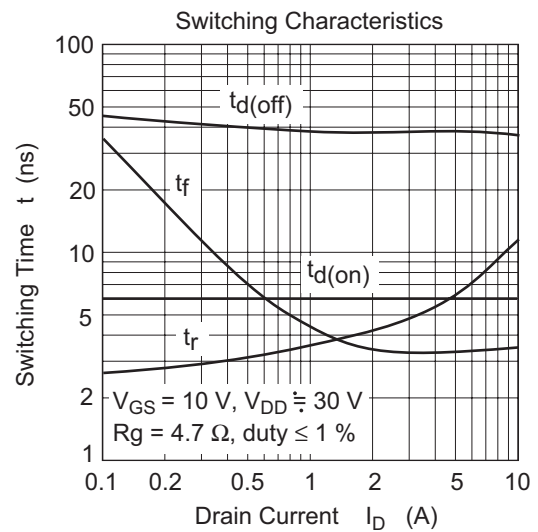
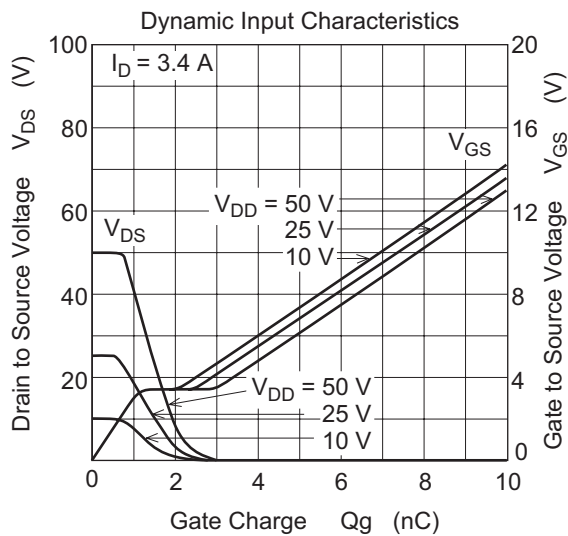
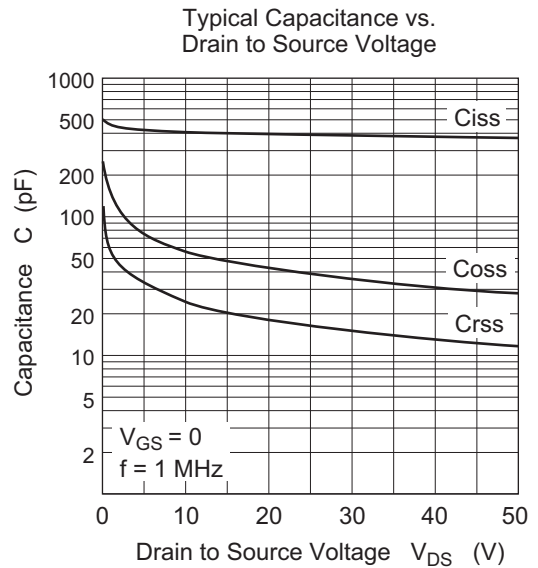
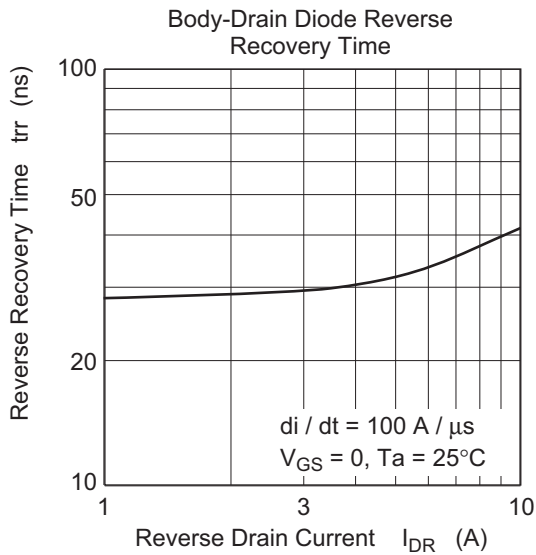
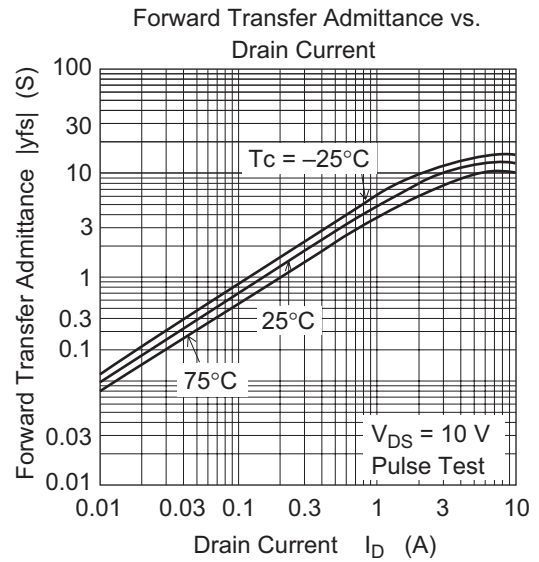
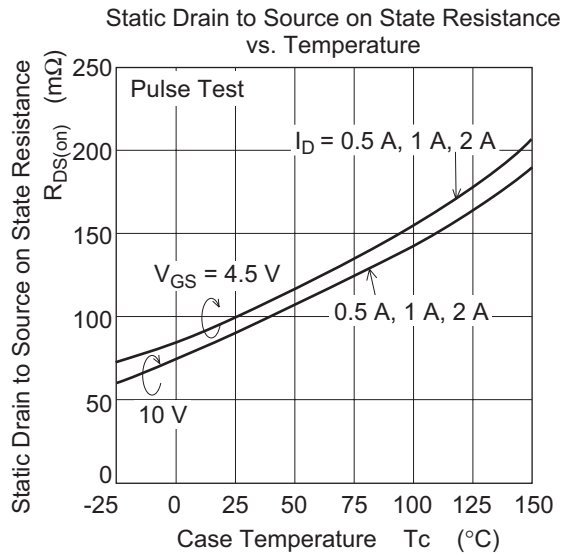
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-80	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	-1	$\mu\text{A}$	$V_{DS} = -80 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$ , $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	165	210	$\text{m}\Omega$	$I_D = -1.3 \text{ A}$ , $V_{GS} = -10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	200	290	$\text{m}\Omega$	$I_D = -1.3 \text{ A}$ , $V_{GS} = -4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	2.0	3.3	—	S	$I_D = -1.3 \text{ A}$ , $V_{DS} = -10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	930	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	$C_{oss}$	—	90	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	56	—	pF	$f = 1 \text{ MHz}$
Total gate charge	$Q_g$	—	16	—	nC	$V_{DD} = -25 \text{ V}$
Gate to source charge	$Q_{gs}$	—	2.1	—	nC	$V_{GS} = -10 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	2.4	—	nC	$I_D = -2.6 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = -10 \text{ V}$ , $I_D = -1.3 \text{ A}$
Rise time	$t_r$	—	12	—	ns	$V_{DD} \approx -30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	40	—	ns	$R_L = 23.0 \Omega$
Fall time	$t_f$	—	5.5	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	$V_{DF}$	—	-0.83	-1.08	V	$I_F = -2.6 \text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	30	—	ns	$I_F = -2.6 \text{ A}$ , $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

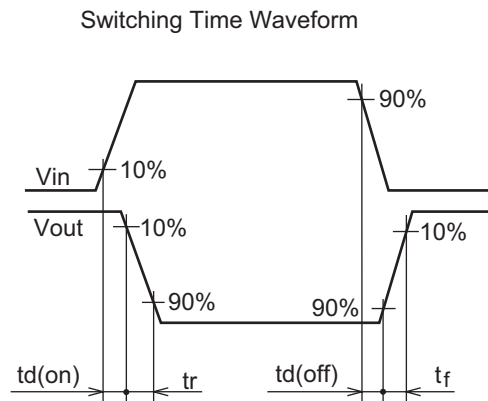
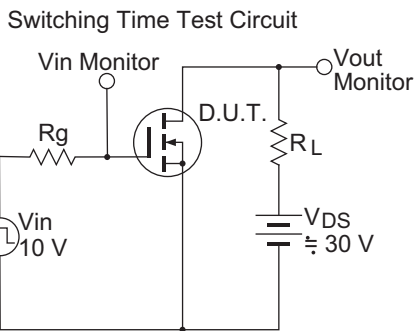
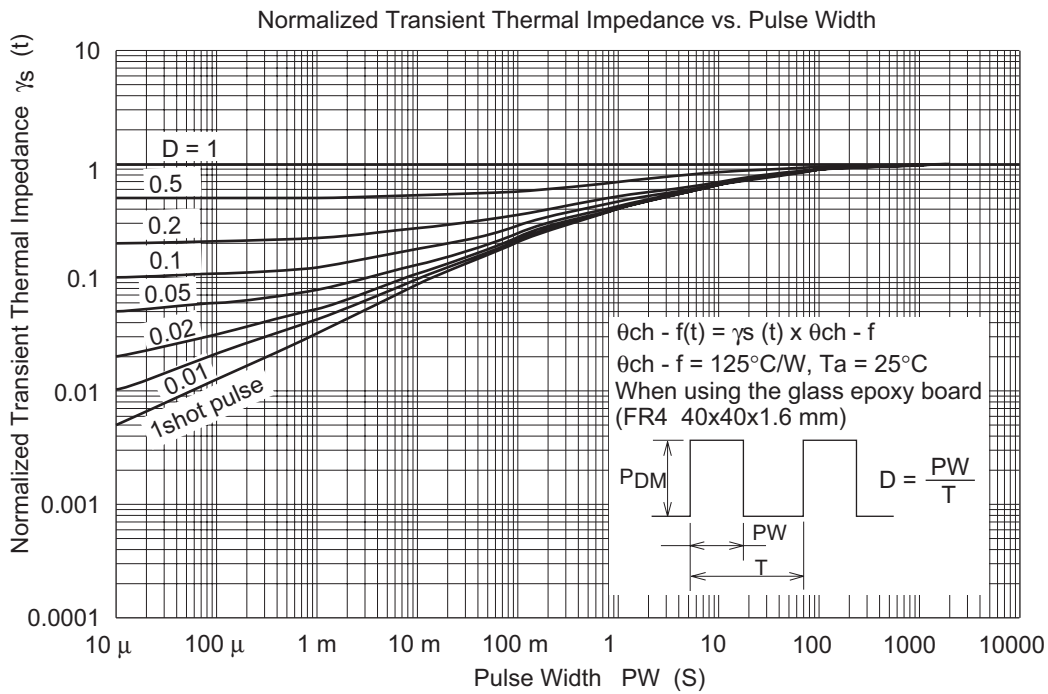
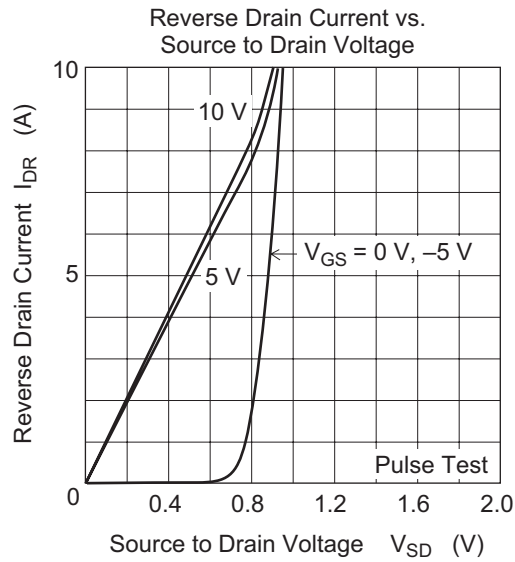
Notes: 4. Pulse test

## Main Characteristics

• N Channel

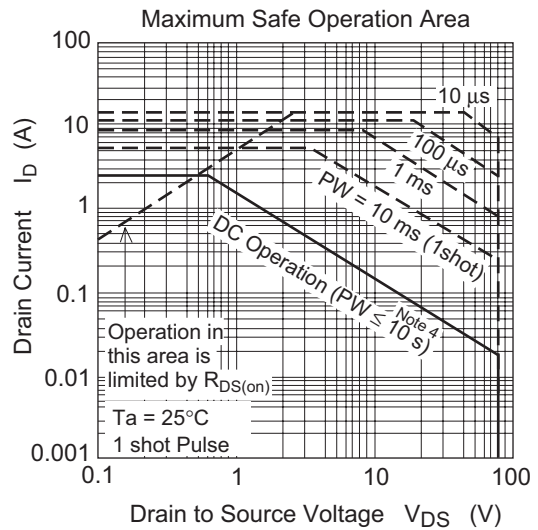
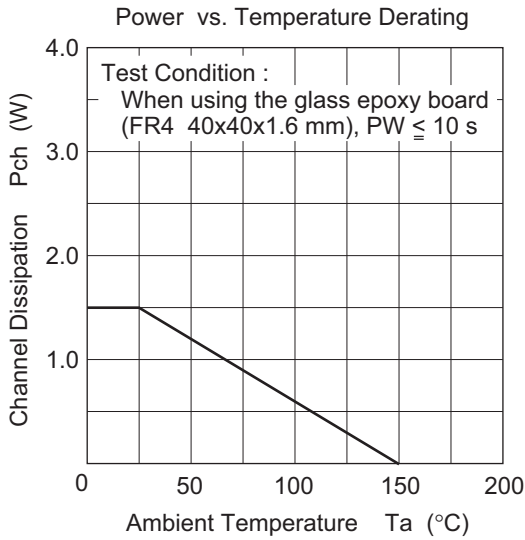




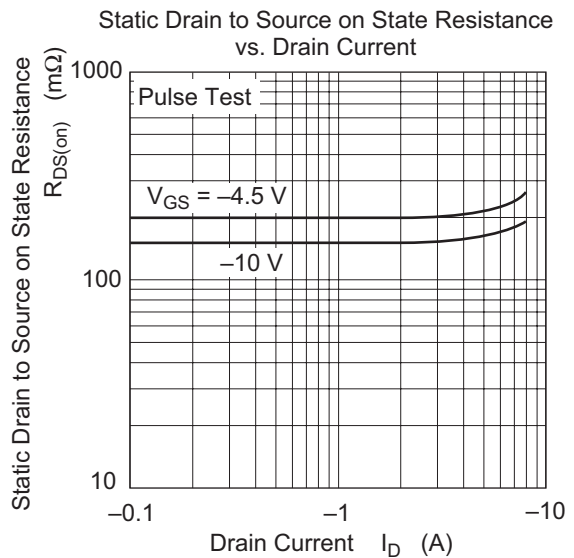
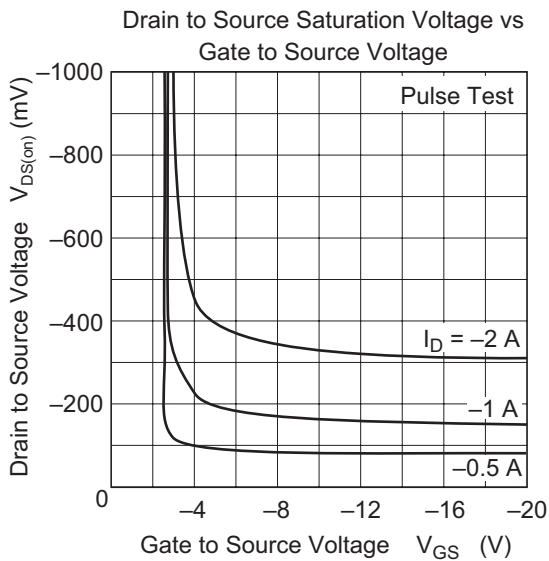
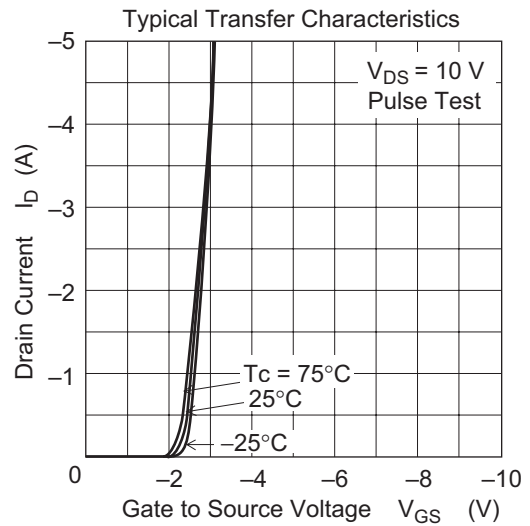
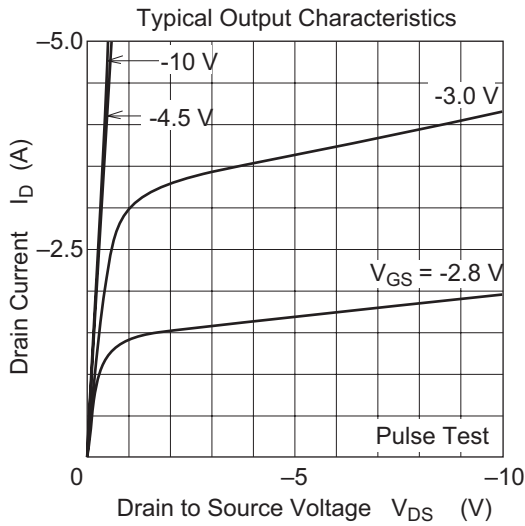


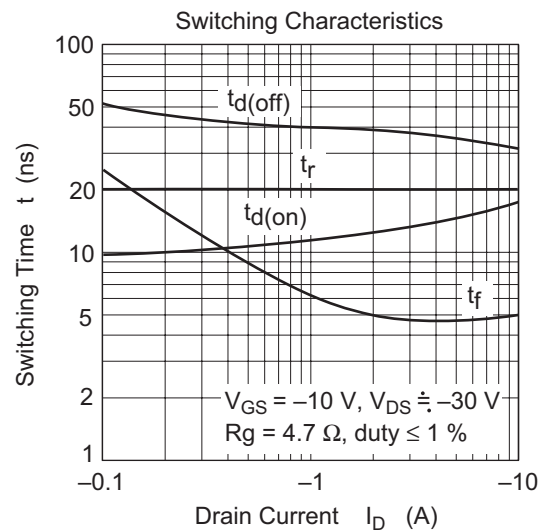
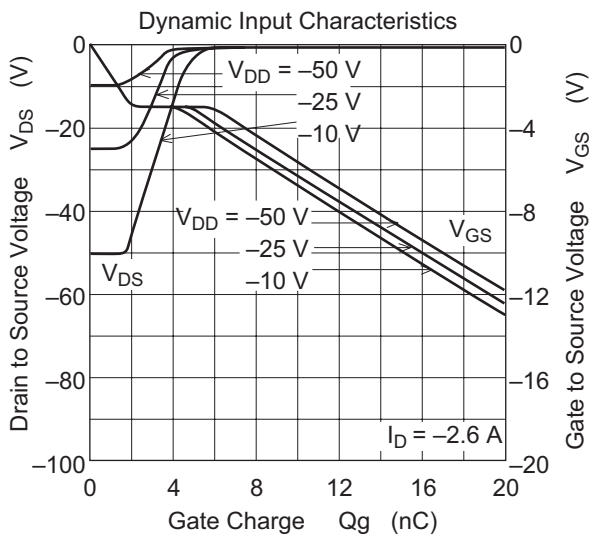
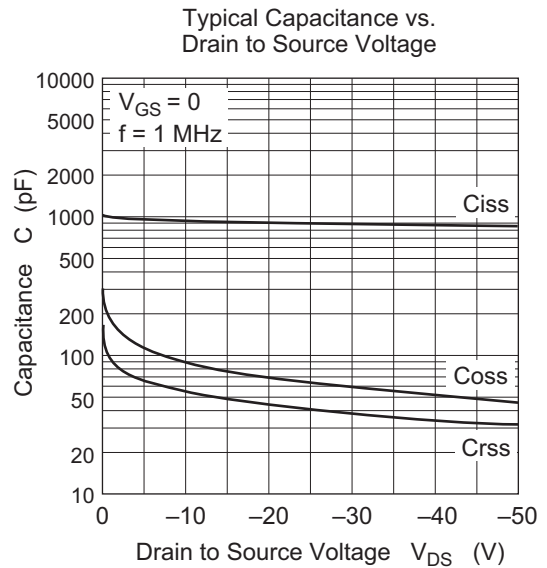
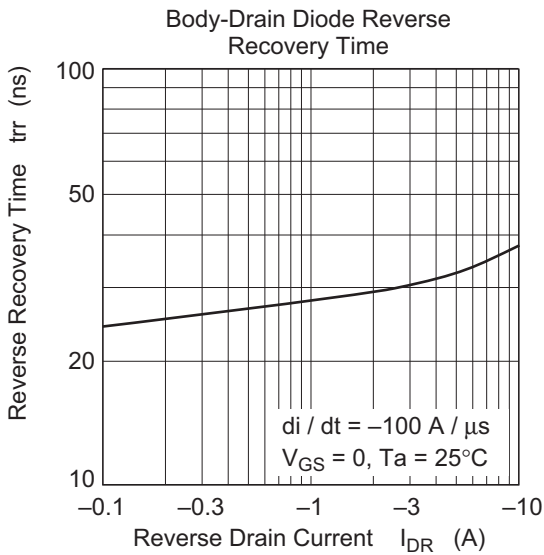
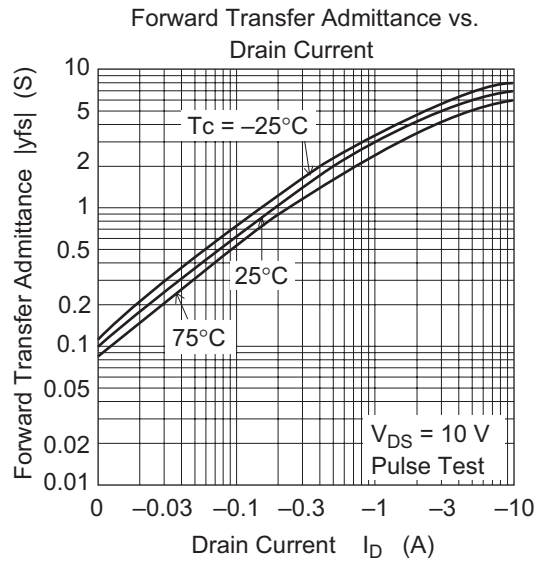
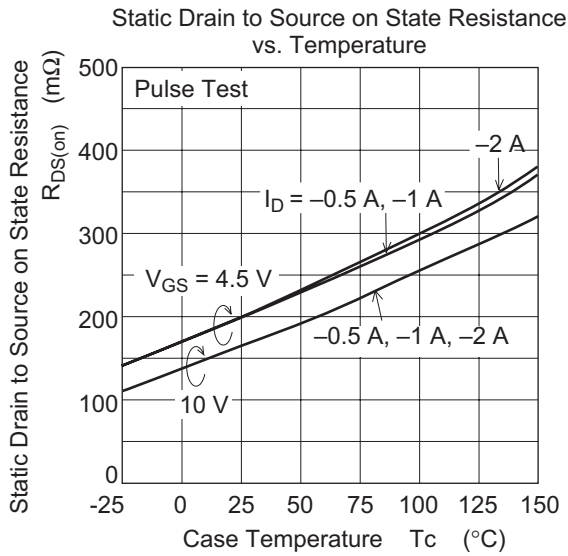


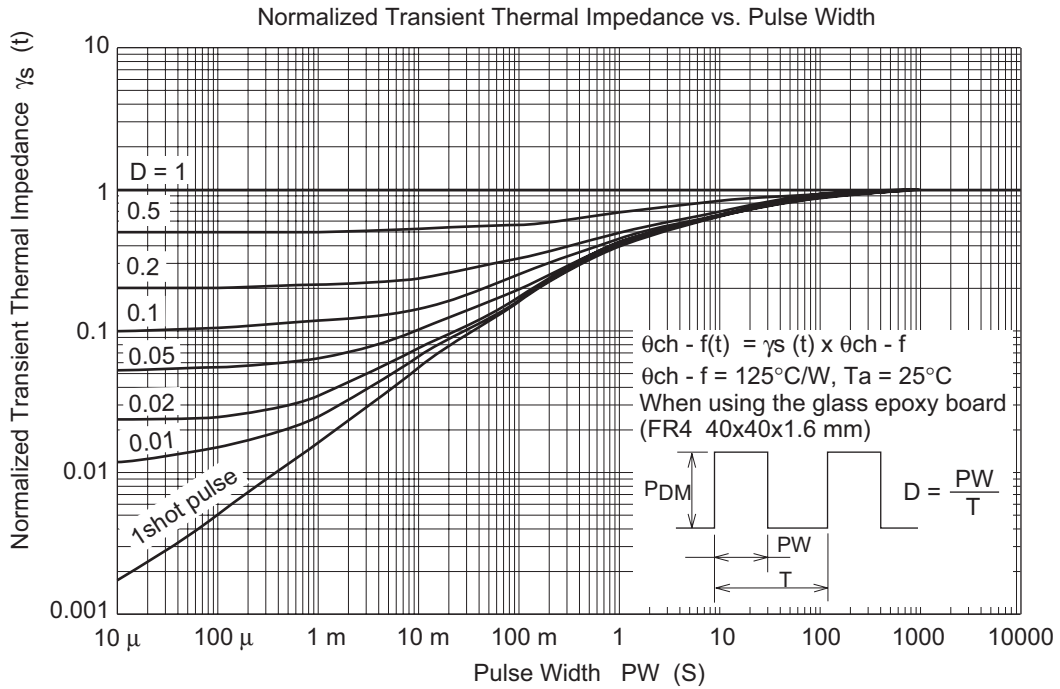
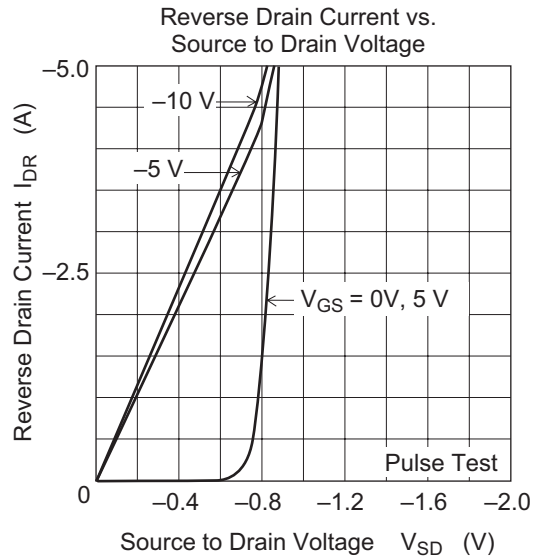
• P Channel



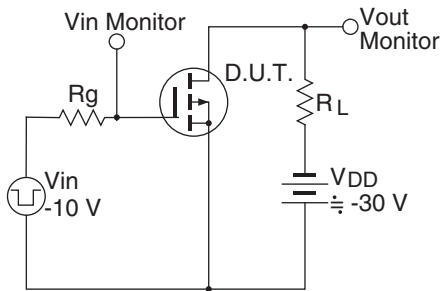
Note 4 :  
When using the glass epoxy board (FR4 40x40x1.6 mm)



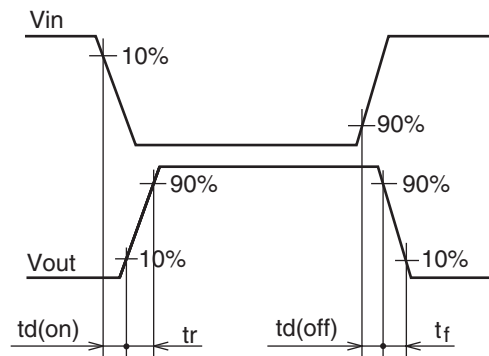




Switching Time Test Circuit

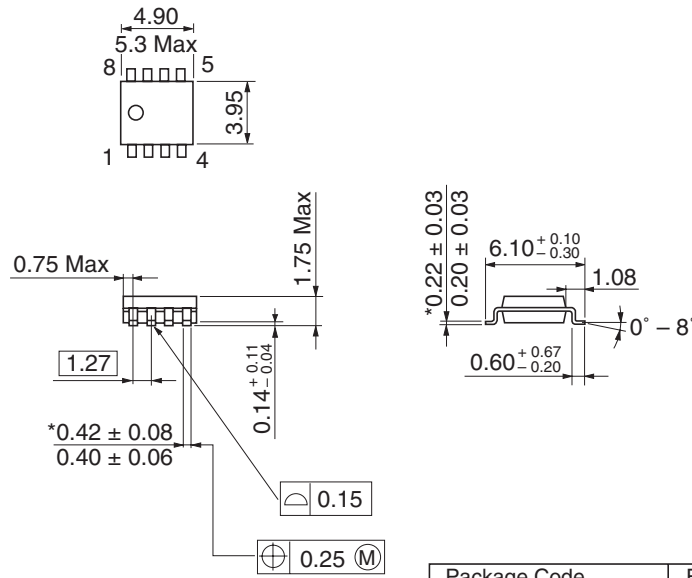


Switching Time Waveform



Package Dimensions

As of January, 2003  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Package Code	FP-8DA
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.085 g

Ordering Information

Part Name	Quantity	Shipping Container
HAT3021R-EL-E	2500 pcs	Taping

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