

## HAT2265H

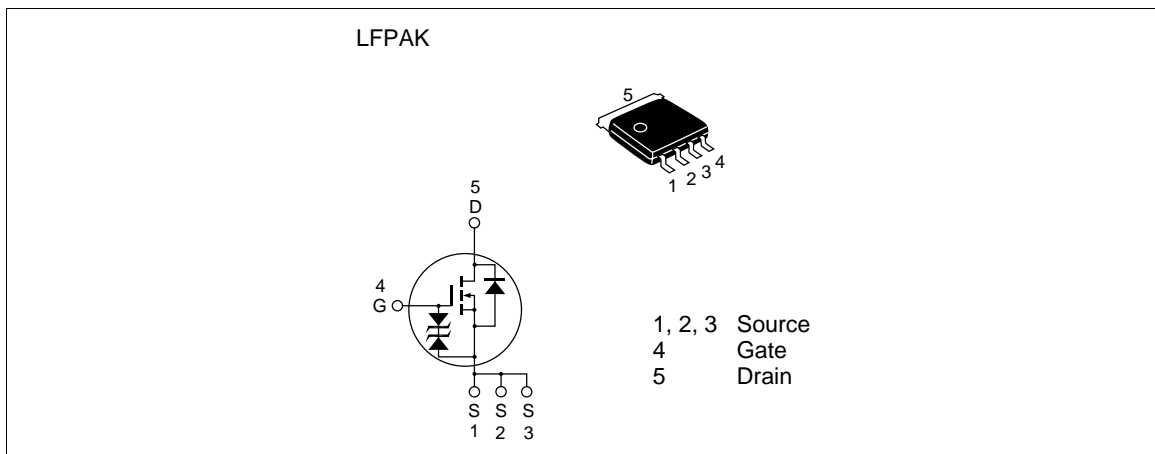
Silicon N Channel Power MOS FET Power Switching

Rev.0.00  
Sept.2004

### Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 2.5 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )
- Lead Free

### Outline



## HAT2265H

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### Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	30	V
Gate to source voltage	V <sub>GSS</sub>	±20	V
Drain current	I <sub>D</sub>	55	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	220	A
Body-drain diode reverse drain current	I <sub>DR</sub>	55	A
Avalanche current	I <sub>AP</sub> <sup>Note 2</sup>	30	A
Avalanche energy	E <sub>AR</sub> <sup>Note 2</sup>	90	mJ
Channel dissipation	P <sub>ch</sub> <sup>Note3</sup>	30	W
Channel to Case Thermal Resistance	θ <sub>ch-C</sub>	4.17	°C/W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%  
2. Value at T<sub>ch</sub> = 25°C, R<sub>g</sub> ≥ 50 Ω  
3. T<sub>c</sub> = 25°C

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### Electrical Characteristics

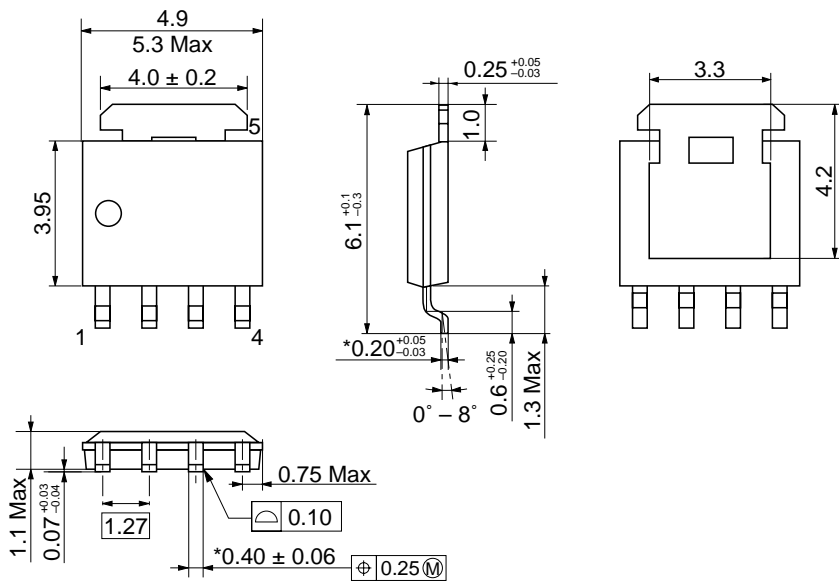
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	$\pm 20$	—	—	V	$I_G = \pm 100 \mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.6	—	2.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.5	3.3	$\text{m}\Omega$	$I_D = 27.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	3.4	5.3	$\text{m}\Omega$	$I_D = 27.5 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	60	100	—	S	$I_D = 27.5 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	5180	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	1200	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	380	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	$R_g$	—	0.5	—	$\Omega$	
Total gate charge	$Q_g$	—	33	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	$Q_{gs}$	—	15	—	nc	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	7.1	—	nc	$I_D = 55 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	13	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 27.5 \text{ A}$
Rise time	$t_r$	—	65	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	$R_L = 0.36 \Omega$
Fall time	$t_f$	—	9.5	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.81	1.06	V	$I_F = 55 \text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	40	—	ns	$I_F = 55 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

Package Dimensions

As of January, 2003  
Unit: mm



\*Ni/Pd/Au plating

Package Code	LFPAK
JEDEC	—
JEITA	—
Mass (reference value)	0.080 g

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Keep safety first in your circuit designs!

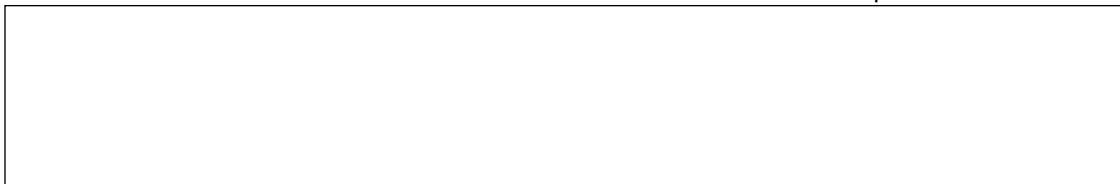
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