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Renesas Electronics website: http://www.renesas.com

April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HAT2220R

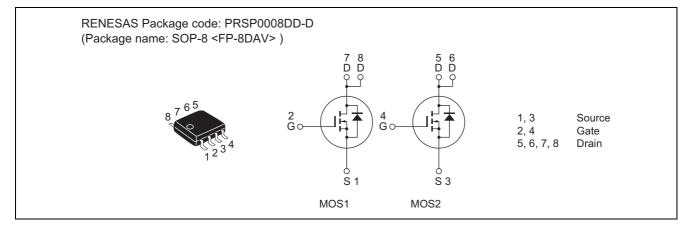
Silicon N Channel MOS FET High Speed Power Switching

> REJ03G1572-0500 Rev.5.00 Jul 20, 2007

Features

- Low on-resistance
- Low drive current
- High density mounting

Outline



Absolute Maximum Ratings

			$(Ta = 25^{\circ}C)$
Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	450	V
Gate to source voltage	V _{GSS}	±30	V
Drain current	ID Note1	0.7	A
Drain peak current	I _{D(pulse)} Note2	2.1	A
Body-drain diode reverse drain current	I _{DR}	0.7	А
Avalanche current	I _{AP} ^{Note3}	0.7	A
Channel dissipation	Pch Note4	2	W
Channel dissipation	Pch Note5	3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1. $PW \le 1 s$

- 2. $PW \le 10 \ \mu s$, duty cycle $\le 1\%$
- 3. STch = 25 °C, Tch \leq 150 °C
- 4. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW \leq 10 s
- 5. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW \leq 10 s

Electrical Characteristics

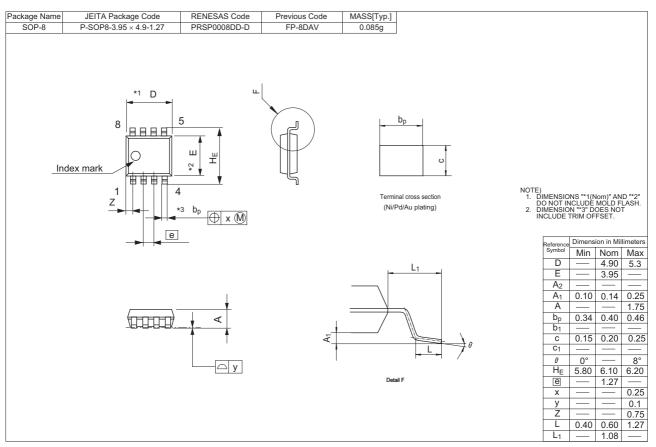
 $(Ta = 25^{\circ}C)$

-			_			(1a - 2JC)
Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR)DSS}	450	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Zero gate voltage drain current	I _{DSS}		_	1	μΑ	$V_{DS} = 450 \text{ V}, V_{GS} = 0$
Gate to source leak current	I _{GSS}		_	±0.1	μA	$V_{GS}=\pm 30~V,~V_{DS}=0$
Gate to source cutoff voltage	V _{GS(off)}	3.0	_	4.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Forward transfer admittance	y _{fs}	0.55	0.95	_	S	$I_D = 0.4 \text{ A}, V_{DS} = 10 \text{ V}^{Note6}$
Static drain to source on state resistance	R _{DS(on)}		5.5	6.5	Ω	$I_D = 0.4 \text{ A}, V_{GS} = 10 \text{ V}^{\text{Note6}}$
Input capacitance	Ciss	_	140	_	pF	V _{DS} = 25 V
Output capacitance	Coss		17	_	pF	V _{GS} = 0 f = 1 MHz
Reverse transfer capacitance	Crss		5	—	pF	
Turn-on delay time	t _{d(on)}	_	22	—	ns	$I_{D} = 0.4 \text{ A} \\ V_{GS} = 10 \text{ V} \\ R_{L} = 562 \Omega \\ Rg = 10 \Omega$
Rise time	tr	—	12	—	ns	
Turn-off delay time	t _{d(off)}		38	_	ns	
Fall time	t _f		47	_	ns	
Total gate charge	Qg		4.9	_	nC	V _{DD} = 360 V
Gate to source charge	Qgs		0.6	—	nC	V _{GS} = 10 V I _D = 0.7 A
Gate to drain charge	Qgd		3.2	_	nC	
Body-drain diode forward voltage	V _{DF}	_	0.84	1.24	V	$I_F = 0.7 \text{ A}, V_{GS} = 0^{Note6}$
Body-drain diode reverse recovery	t _{rr}	_	120	_	ns	$I_F = 0.7 \text{ A}, V_{GS} = 0$
time						di _F /dt = 100 A/ μs

Notes: 6. Pulse test

 Since this device includes two high voltage Power MOS FET chips (V_{DSS} ≥ 450 V), high voltage margin may occur. (Between No.6 pin and No.7 pin in the outline fig.) Therefore, please be sure to confirm about Electric discharge between No.6 pin and No.7 pin in the equivalent circuit.

Package Dimensions



Ordering Information

Part No.	Quantity	Shipping Container
HAT2220R-EL-E	2500 pcs	Taping

RenesasTechnology Corp. sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

- Benesas lechnology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
 Pines
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