To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HAT2210R, HAT2210RJ

Silicon N Channel Power MOS FET with Schottky Barrier Diode
High Speed Power Switching

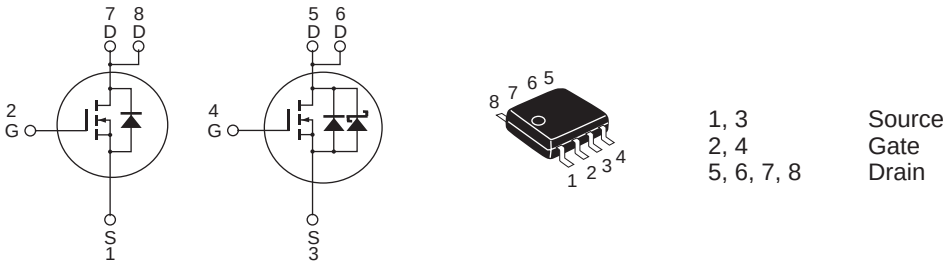
REJ03G0578-0300
Rev.3.00
Mar.15.2005

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Built-in Schottky Barrier Diode

Outline

RENESAS Package code: PRSP0008DD-A
(Package name: SOP-8<FP-8DA>)



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings				Unit
		HAT2210R		HAT2210RJ		
		MOS1	MOS2 & SBD	MOS1	MOS2 & SBD	
Drain to source voltage	V_{DSS}	30	30	30	30	V
Gate to source voltage	V_{GSS}	±20	±12	±20	±12	V
Drain current	I_D	7.5	8.0	7.5	8.0	A
Drain peak current	$I_{D(pulse)}$ Note1	60	64	60	64	A
Reverse drain current	I_{DR}	7.5	8.0	7.5	8.0	A
Avalanche current	I_{AP} Note 2	—	—	7.5	8.0	A
Avalanche energy	E_{AR} Note 2	—	—	5.62	6.4	mJ
Channel dissipation	Pch Note3	1.5	1.5	1.5	1.5	W
Channel temperature	Tch	150	150	150	150	°C
Storage temperature	Tstg	–55 to +150	–55 to +150	–55 to +150	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, duty cycle ≤ 1 %
2. Value at Tch = 25°C, Rg ≥ 50 Ω
3. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s

Electrical Characteristics

- **MOS1**

(Ta = 25°C)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current		I_{GSS}	—	—	±0.1	µA	V_{GS} = ±20 V, V_{DS} = 0
Zero gate voltage drain current		I_{DSS}	—	—	1	µA	V_{DS} = 30 V, V_{GS} = 0
Zero gate voltage drain current	HAT2210R	I_{DSS}	—	—	—	µA	V_{DS} = 24 V, V_{GS} = 0, Ta = 125°C
	HAT2210RJ	I_{DSS}	—	—	10	µA	
Gate to source cutoff voltage		$V_{GS(off)}$	1.0	—	2.5	V	V_{DS} = 10 V, I_D = 1 mA
Static drain to source on state resistance		$R_{DS(on)}$	—	19	24	mΩ	I_D = 3.75 A, V_{GS} = 10 V Note4
		$R_{DS(on)}$	—	27	40	mΩ	I_D = 3.75 A, V_{GS} = 4.5 V Note4
Forward transfer admittance		$\|y_{fs}\|$	9	15	—	S	I_D = 3.75 A, V_{DS} = 10 V Note4
Input capacitance		Ciss	—	630	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1MHz
Output capacitance		Coss	—	155	—	pF	
Reverse transfer capacitance		Crss	—	57	—	pF	
Total gate charge		Qg	—	4.6	—	nC	V_{DD} = 10 V, V_{GS} = 4.5 V, I_D = 7.5 A
Gate to source charge		Qgs	—	2.2	—	nC	
Gate to drain charge		Qgd	—	1.2	—	nC	
Turn-on delay time		$t_{d(on)}$	—	7	—	ns	V_{GS} =10 V, I_D = 3.75 A, V_{DD} ≈ 10 V, R_L = 2.66 Ω, R_g = 4.7 Ω
Rise time		t_r	—	14	—	ns	
Turn-off delay time		$t_{d(off)}$	—	36	—	ns	
Fall time		t_f	—	3.4	—	ns	
Body–drain diode forward voltage		V_{DF}	—	0.85	1.11	V	IF = 7.5 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time		t_{rr}	—	17	—	ns	IF =7.5 A, V_{GS} = 0 diF/ dt = 100 A/µs

Notes: 4. Pulse test

- **MOS2 & Schottky Barrier Diode**

(Ta = 25°C)

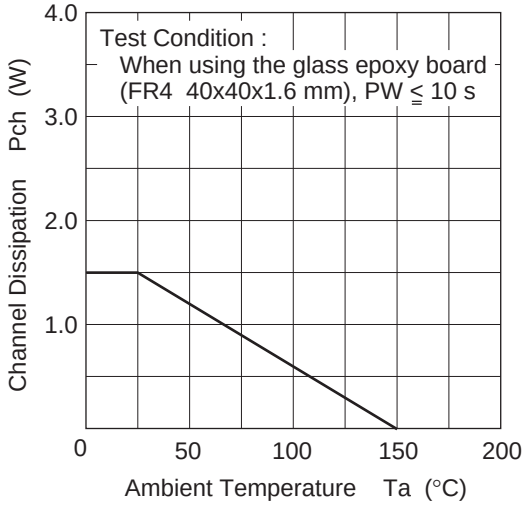
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source leak current	I_{GSS}	—	—	±0.1	µA	V_{GS} = ±12 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	1	mA	V_{DS} = 30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.4	—	2.5	V	V_{DS} = 10 V, I_D =1 mA
Static drain to source on state resistance	$R_{DS(on)}$	—	17	22	mΩ	I_D =4 A, V_{GS} = 10 V Note4
	$R_{DS(on)}$	—	21	29	mΩ	I_D = 4 A, V_{GS} = 4.5 V Note4
Forward transfer admittance	$\|y_{fs}\|$	15	25	—	S	I_D = 4 A, V_{DS} = 10 V Note4
Input capacitance	Ciss	—	1330	—	pF	V_{DS} = 10 V, V_{GS} = 0, f = 1MHz
Output capacitance	Coss	—	230	—	pF	
Reverse transfer capacitance	Crss	—	92	—	pF	
Total gate charge	Qg	—	11	—	nC	V_{DD} = 10 V, V_{GS} = 4.5 V, I_D = 8 A
Gate to source charge	Qgs	—	3.8	—	nC	
Gate to drain charge	Qgd	—	3.2	—	nC	
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	V_{GS} = 10 V, I_D = 4 A, V_{DD} ≈ 10 V, R_L = 2.5 Ω, R_g = 4.7 Ω
Rise time	t_r	—	16	—	ns	
Turn-off delay time	$t_{d(off)}$	—	43	—	ns	
Fall time	t_f	—	3.9	—	ns	
Schottky Barrier diode forward voltage	V_F	—	0.5	—	V	IF = 3.5 A, V_{GS} = 0 Note4
Body–drain diode reverse recovery time	t_{rr}	—	15	—	ns	IF = 8 A, V_{GS} = 0 diF/ dt = 100 A/µs

Notes: 4. Pulse test

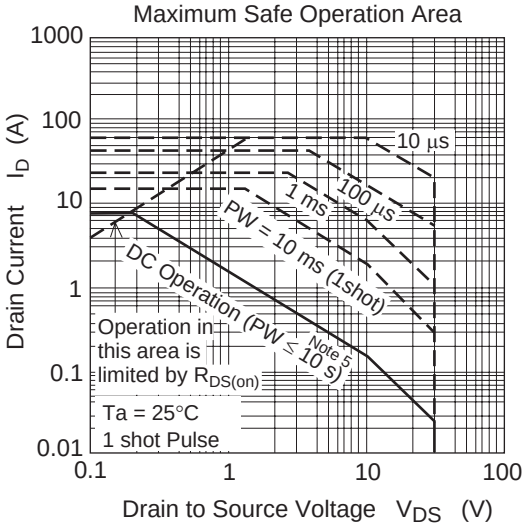
Main Characteristics

• **MOS1**

Power vs. Temperature Derating

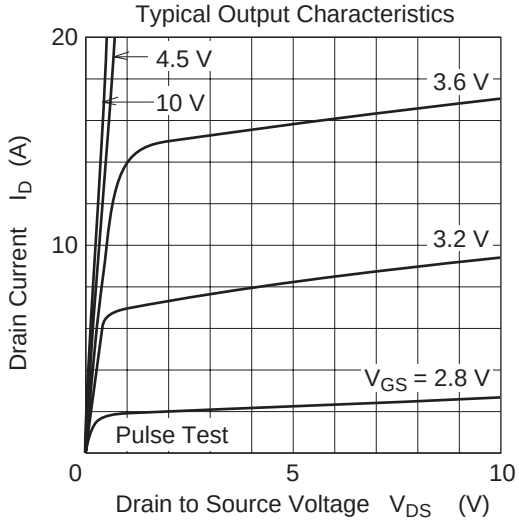


Maximum Safe Operation Area

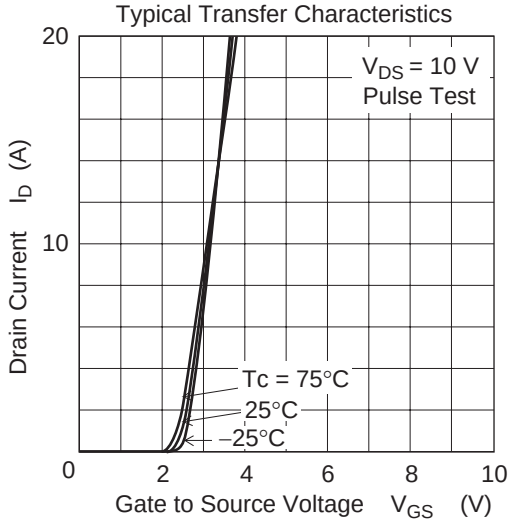


Note 5 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

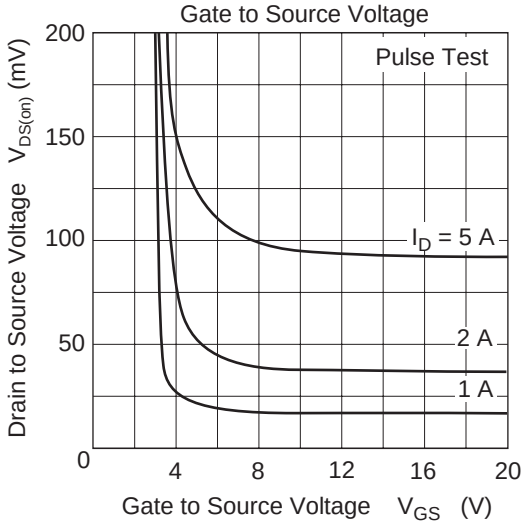
Typical Output Characteristics



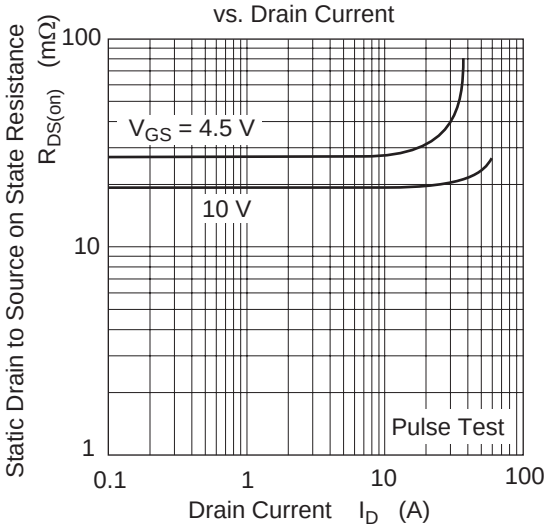
Typical Transfer Characteristics



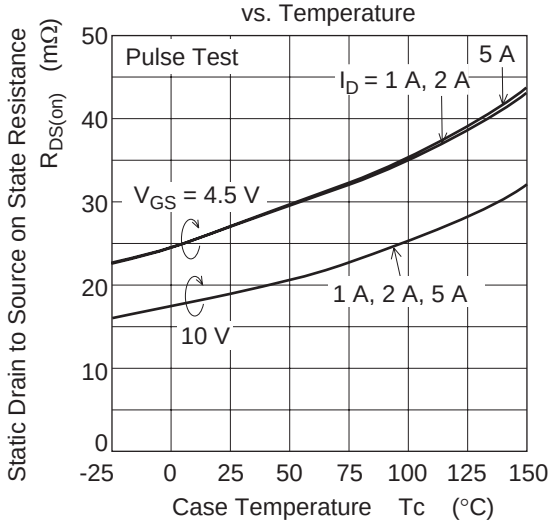
Drain to Source Saturation Voltage vs
Gate to Source Voltage



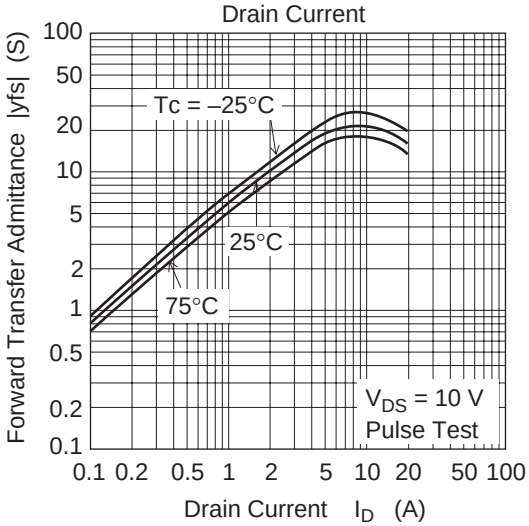
Static Drain to Source on State Resistance
vs. Drain Current



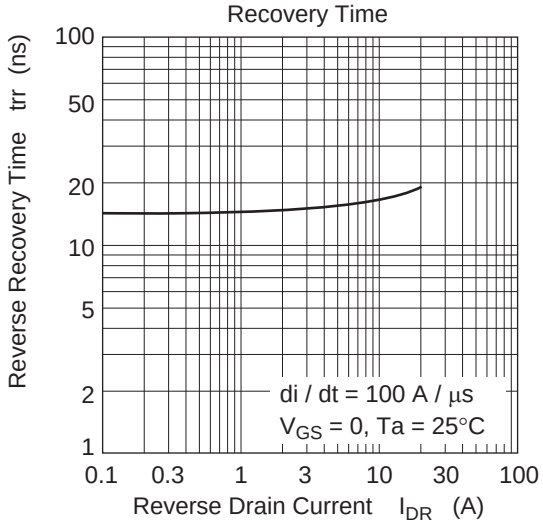
Static Drain to Source on State Resistance vs. Temperature



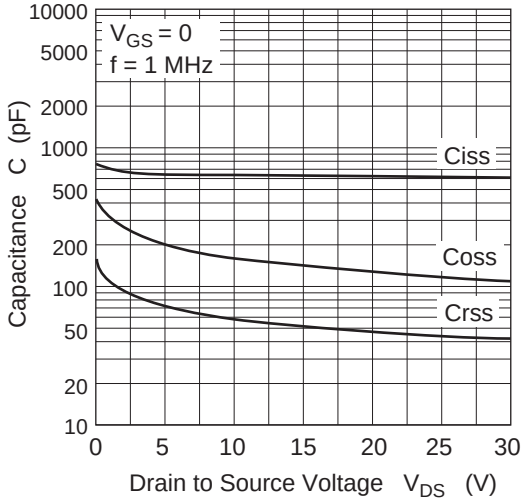
Forward Transfer Admittance vs. Drain Current



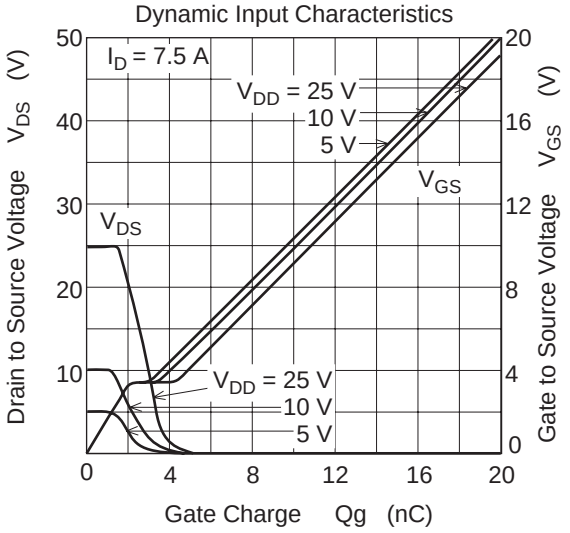
Body-Drain Diode Reverse Recovery Time



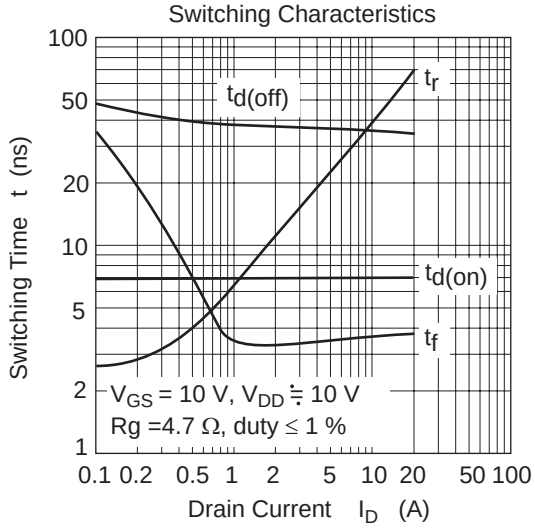
Typical Capacitance vs. Drain to Source Voltage



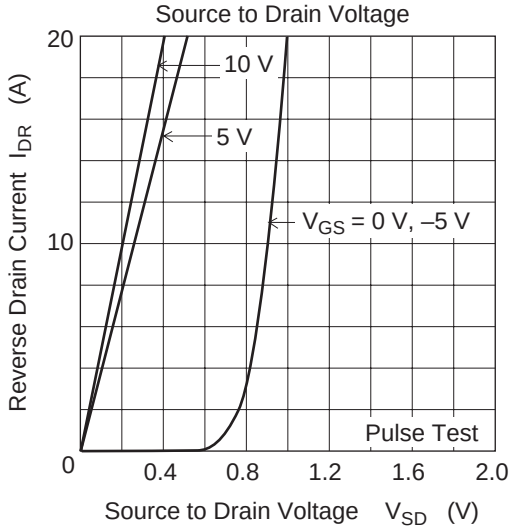
Dynamic Input Characteristics



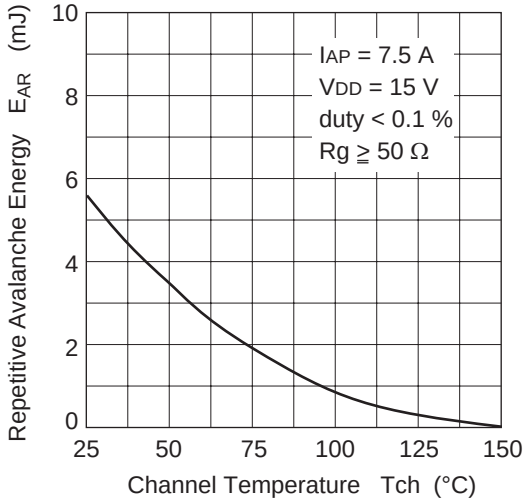
Switching Characteristics



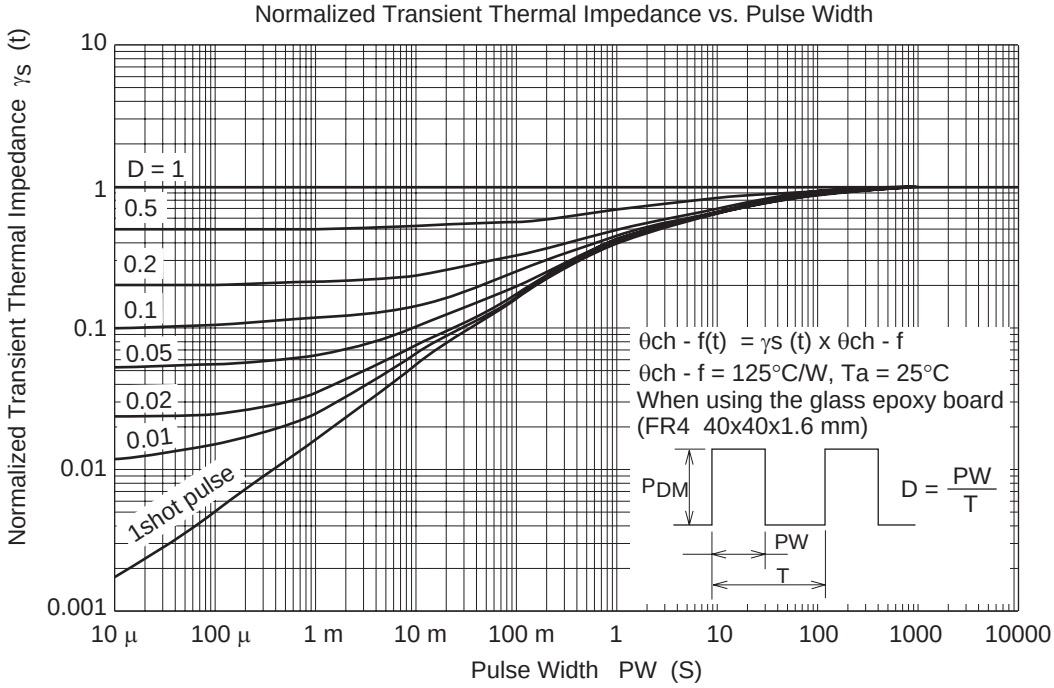
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

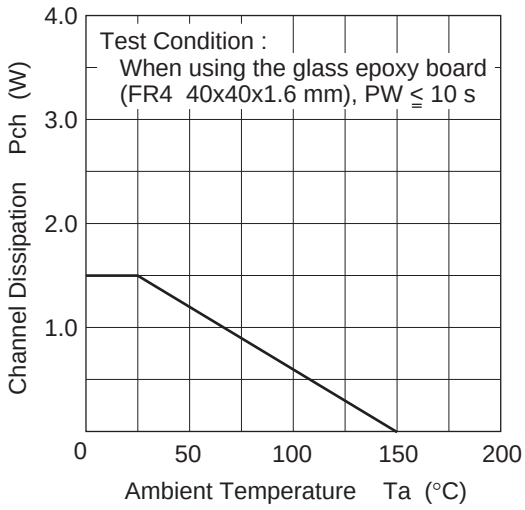


Normalized Transient Thermal Impedance vs. Pulse Width

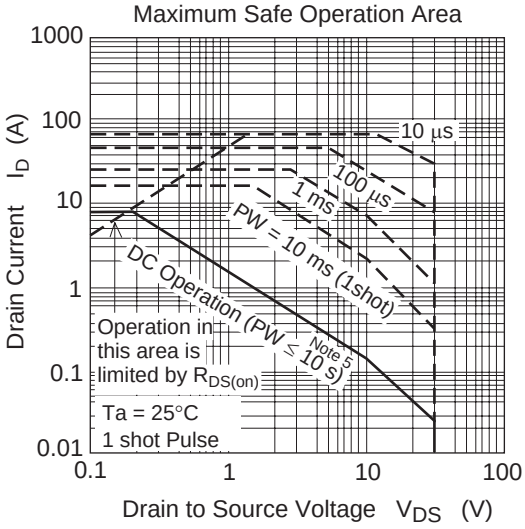


• MOS2 & Schottky Barrier Diode

Power vs. Temperature Derating

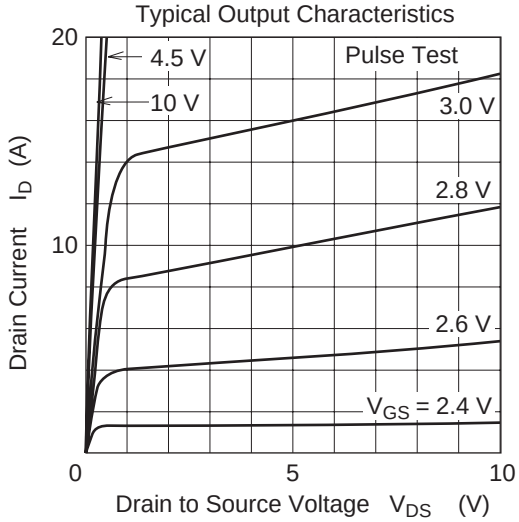


Maximum Safe Operation Area

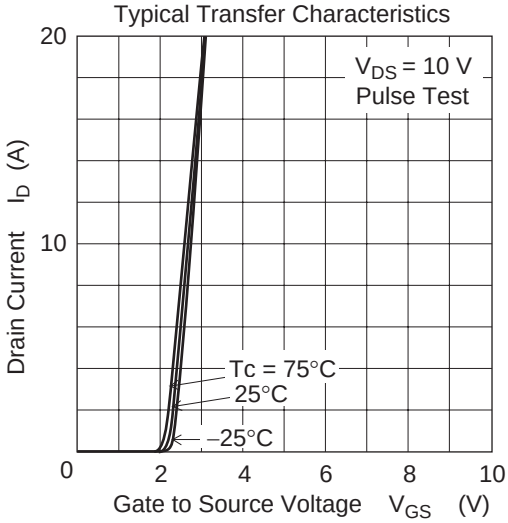


Note 5 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)

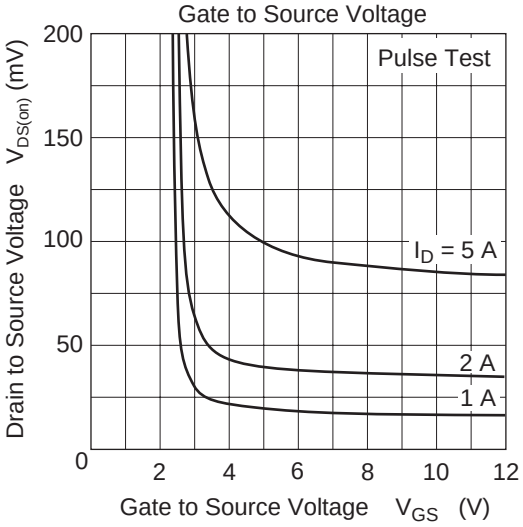
Typical Output Characteristics



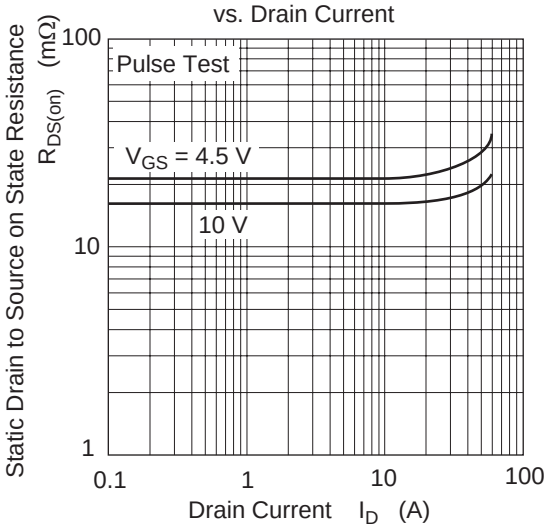
Typical Transfer Characteristics



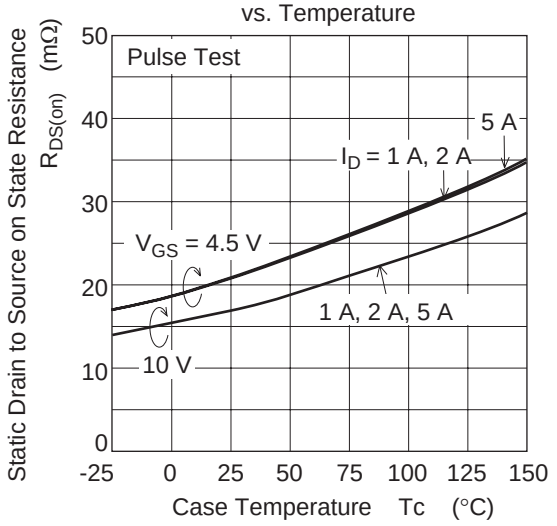
Drain to Source Saturation Voltage vs Gate to Source Voltage



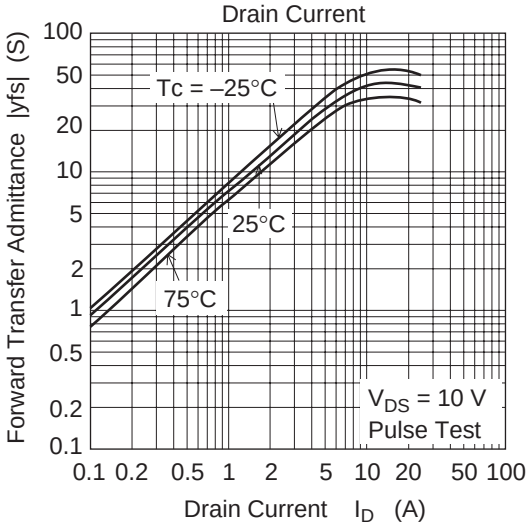
Static Drain to Source on State Resistance vs. Drain Current



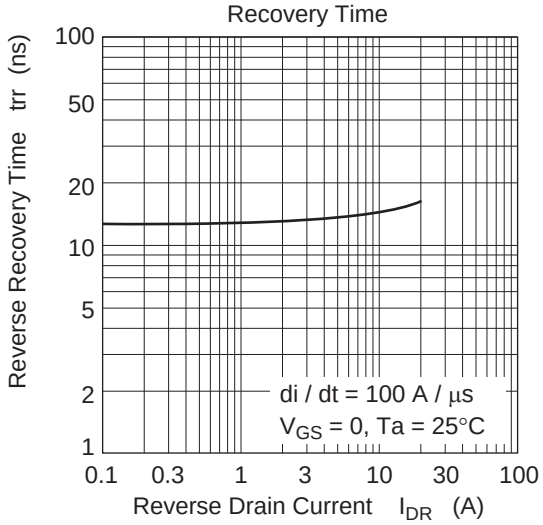
Static Drain to Source on State Resistance vs. Temperature



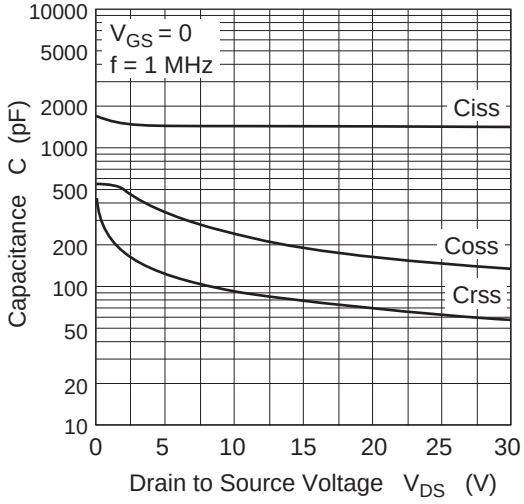
Forward Transfer Admittance vs. Drain Current



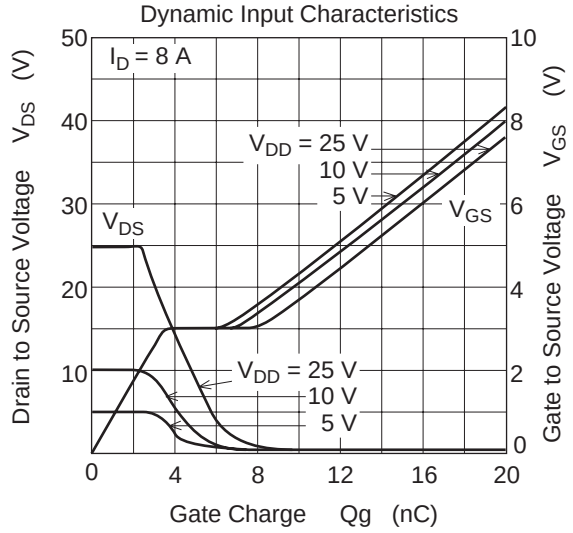
Body-Drain Diode Reverse Recovery Time



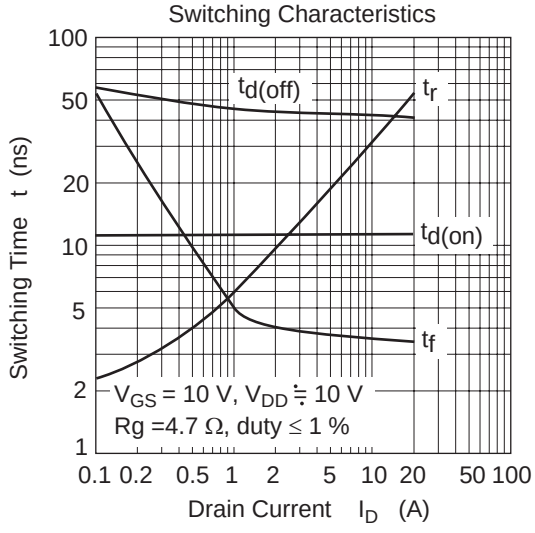
Typical Capacitance vs. Drain to Source Voltage



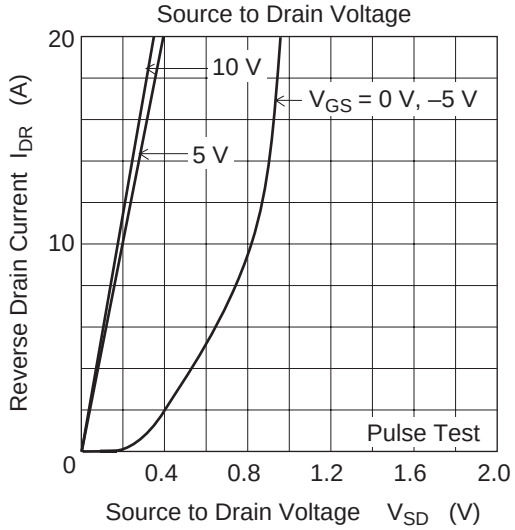
Dynamic Input Characteristics



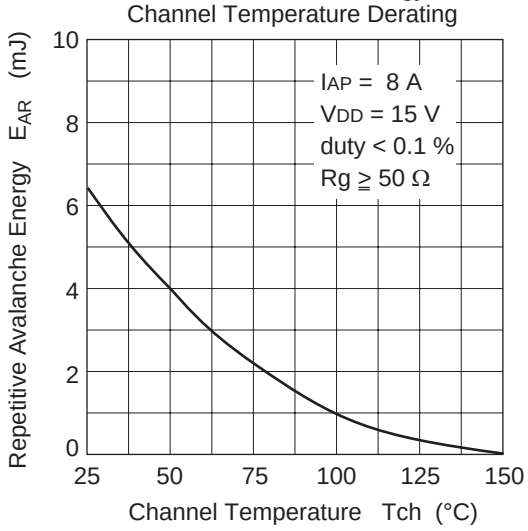
Switching Characteristics



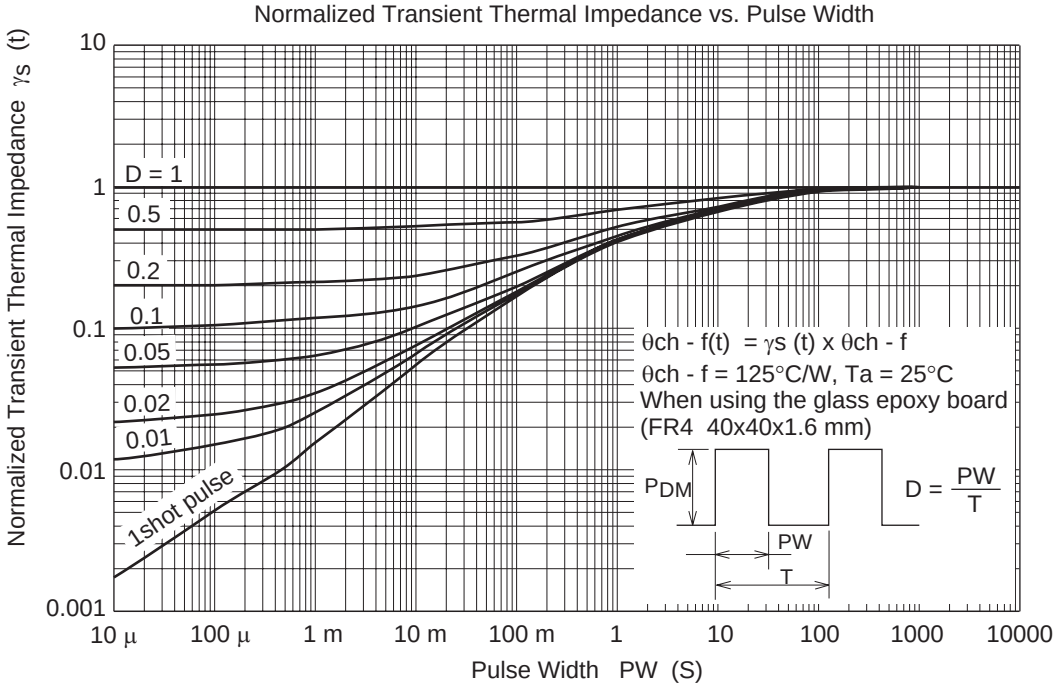
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

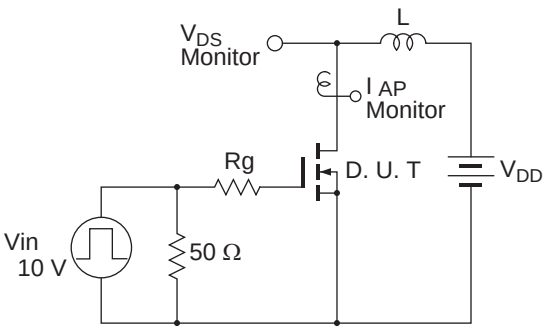


Normalized Transient Thermal Impedance vs. Pulse Width



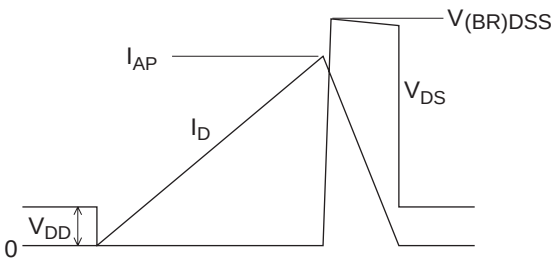
• **Common**

Avalanche Test Circuit

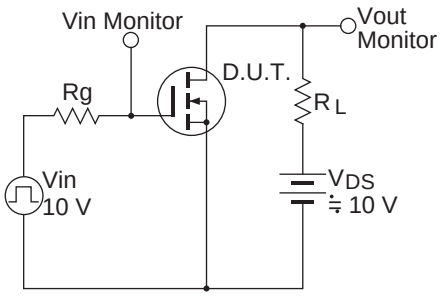


Avalanche Waveform

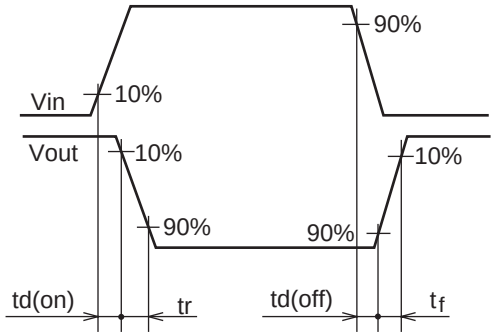
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

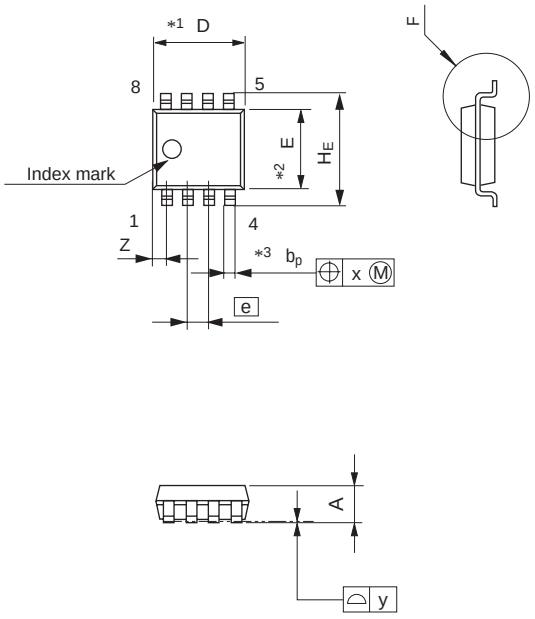


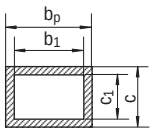
Switching Time Waveform



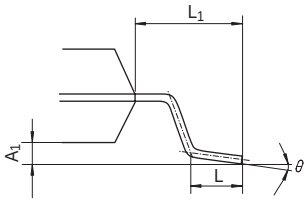
Package Dimensions

JEITA Package Code	RENESAS Code	Package Name	MASS[Typ.]
P-SOP8-3.95 × 4.9-1.27	PRSP0008DD-A	FP-8DA	0.085g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1(Nom)" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	4.90	5.3
E	—	3.95	—
A_2	—	—	—
A_1	0.10	0.14	0.25
A	—	—	1.75
b_p	0.34	0.42	0.50
b_1	—	0.40	—
c	0.19	0.22	0.25
c_1	—	0.20	—
θ	0°	—	8°
H_E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.1
Z	—	—	0.75
L	0.40	0.60	1.27
L_1	—	1.08	—

Ordering Information

Part Name	Quantity	Shipping Container
HAT2210R-EL-E	2500 pcs	Taping
HAT2210RJ-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon .2.0