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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HAT1094C

Silicon P Channel MOS FET Power Switching

REJ03G1231-0400

Rev.4.00

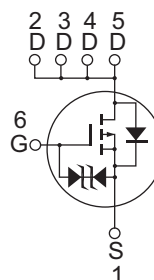
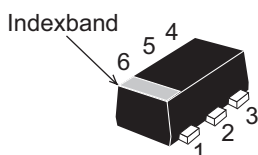
Feb 28, 2006

Features

- Low on-resistance
 $R_{DS(on)} = 67 \text{ m}\Omega$ typ. (at $V_{GS} = -4.5 \text{ V}$)
- Low drive current.
- 1.8 V gate drive devices.
- High density mounting

Outline

RENESAS Package code: PWSF0006JA-A
(Package name: CMFPAK-6)



1. Source
2. Drain
3. Drain
4. Drain
5. Drain
6. Gate

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source voltage	V_{DSS}	-12	V
Gate to Source voltage	V_{GSS}	± 8	V
Drain current	I_D	-2.5	A
Drain peak current	I_D (pulse) ^{Note 1}	-10	A
Body - Drain diode reverse drain current	I_{DR}	-2.5	A
Channel dissipation	P_{ch} ^{Note 2}	850	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board. (FR4 $40 \times 40 \times 1.6\text{mm}$), $T_a = 25^\circ\text{C}$

Electrical Characteristics

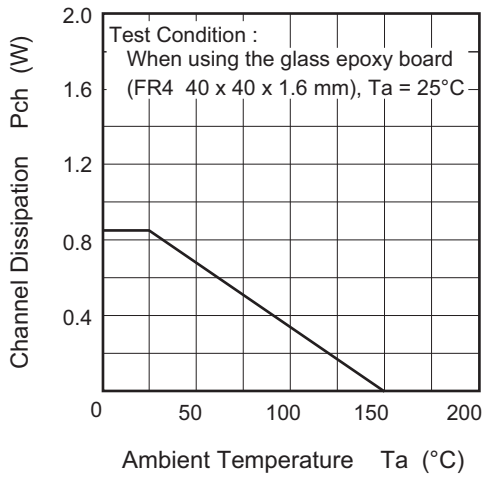
(Ta = 25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain to Source breakdown voltage	$V_{(BR)DSS}$	-12	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to Source breakdown voltage	$V_{(BR)GSS}$	± 8	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to Source leakage current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 6.4 \text{ V}$, $V_{DS} = 0$
Drain to Source leakage current	I_{DSS}	—	—	-1	μA	$V_{DS} = -12 \text{ V}$, $V_{GS} = 0$
Gate to Source cutoff voltage	$V_{GS(th)}$	-0.3	—	-1.2	V	$I_D = -1 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Drain to Source on state resistance	$R_{DS(on)}$	—	67	88	m Ω	$I_D = -1.3 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note3}
		—	90	126	m Ω	$I_D = -1.3 \text{ A}$, $V_{GS} = -2.5 \text{ V}$ ^{Note3}
		—	128	192	m Ω	$I_D = -1.3 \text{ A}$, $V_{GS} = -1.8 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	3.5	5	—	S	$I_D = -1.3 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	530	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	130	—	pF	
Reverse transfer capacitance	C_{rss}	—	95	—	pF	
Total gate charge	Q_g	—	6.5	—	nC	$V_{DS} = -10 \text{ V}$, $V_{GS} = -4.5 \text{ V}$, $I_D = -2.5 \text{ A}$
Gate to Source charge	Q_{gs}	—	1	—	nC	
Gate to Drain charge	Q_{gd}	—	1.8	—	nC	
Turn - on delay time	$t_{d(on)}$	—	12	—	ns	$V_{DS} = -10 \text{ V}$, $V_{GS} = -4.5 \text{ V}$, $I_D = -1.3 \text{ A}$, $R_L = 7.7 \text{ }\Omega$, $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	52	—	ns	
Turn - off delay time	$t_{d(off)}$	—	62	—	ns	
Fall time	t_f	—	9	—	ns	
Body - Drain diode forward voltage	V_{DF}	—	-0.85	-1.1	V	$I_F = -2.5 \text{ A}$, $V_{GS} = 0$

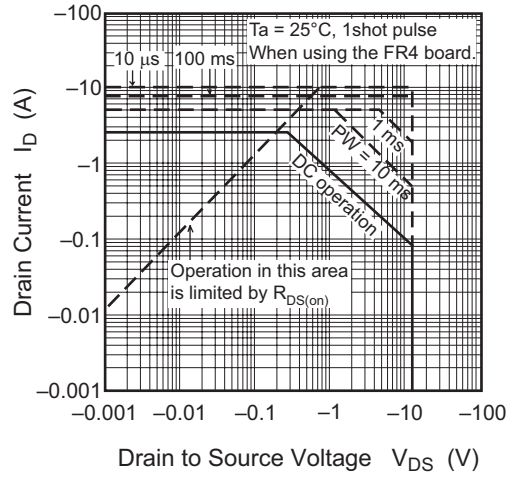
Notes: 3. Pulse test

Main Characteristics

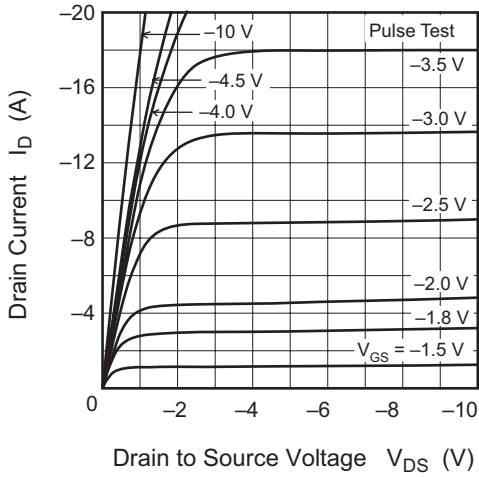
Power vs. Temperature Derating



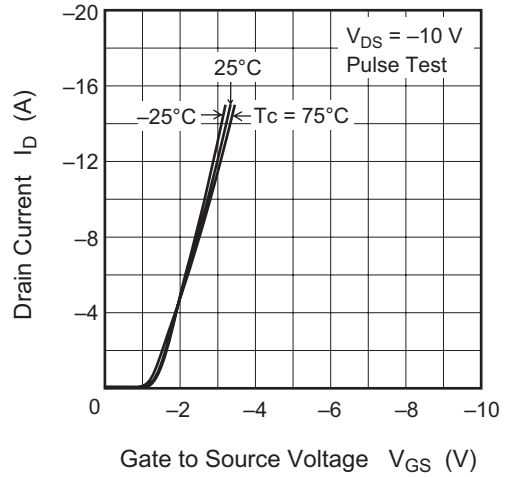
Maximum Safe Operation Area



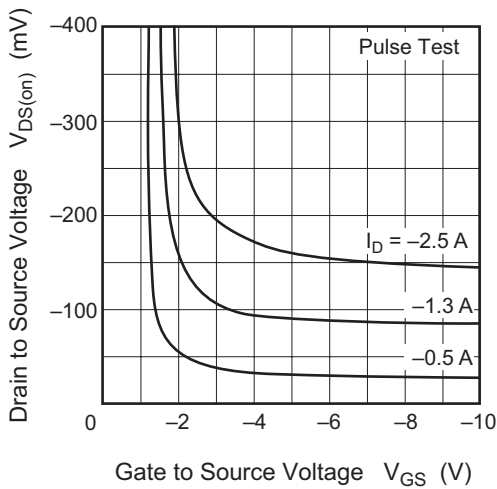
Typical Output Characteristics



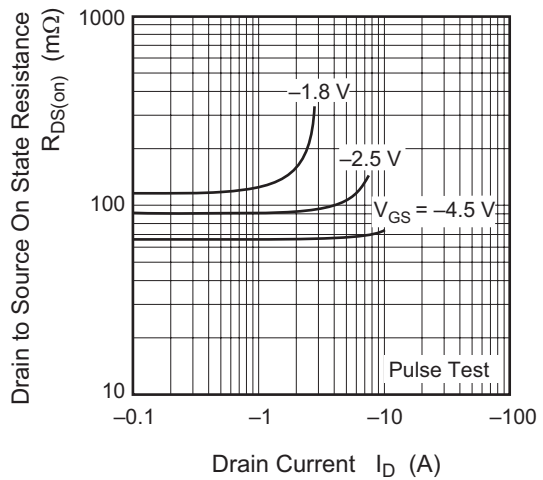
Typical Transfer Characteristics

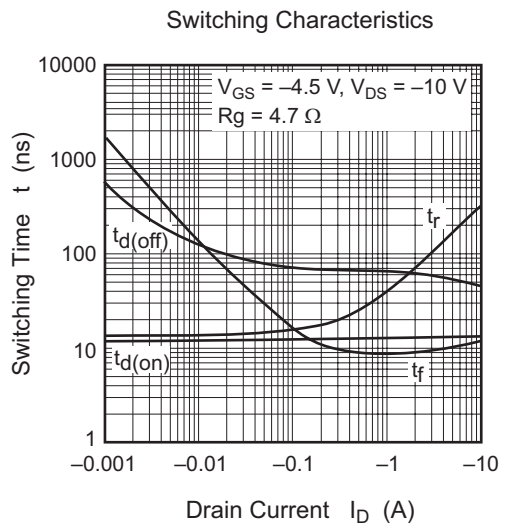
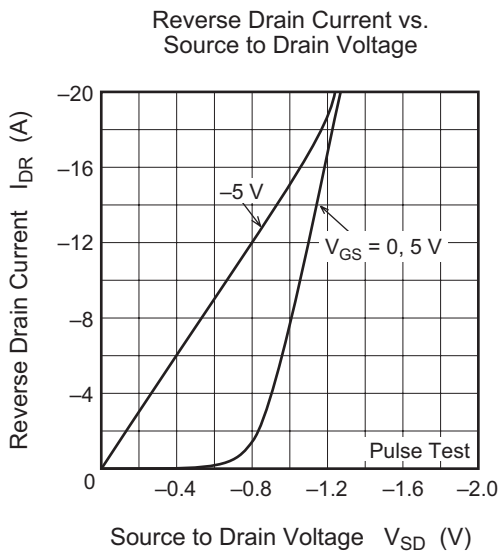
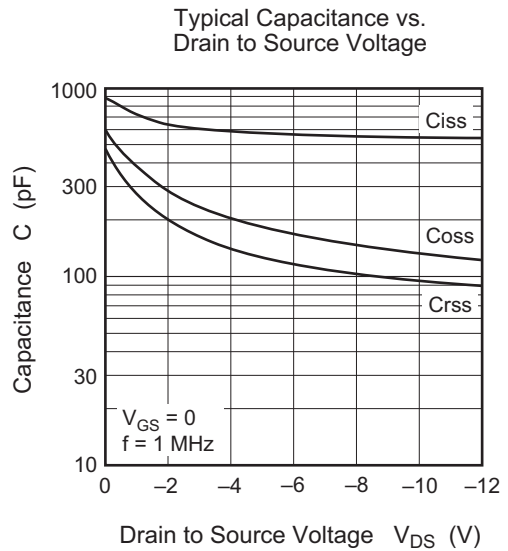
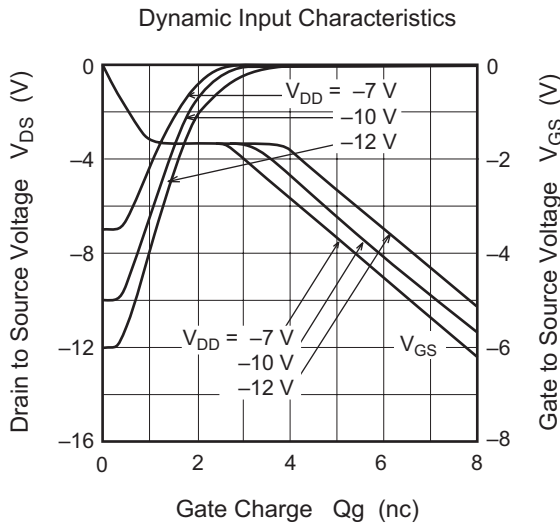
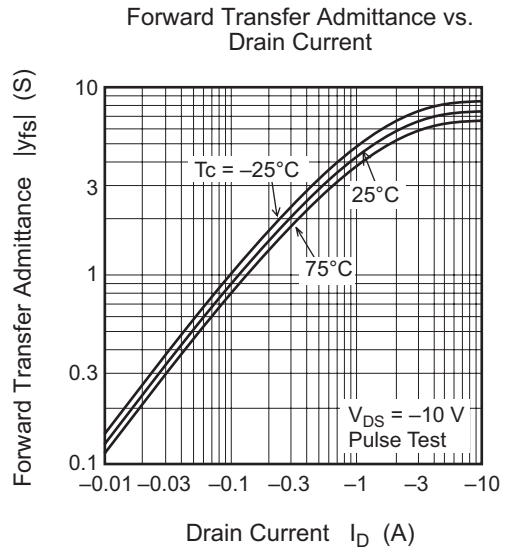
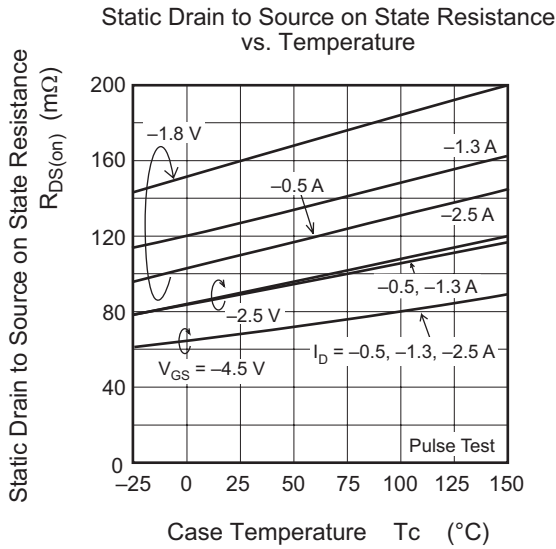


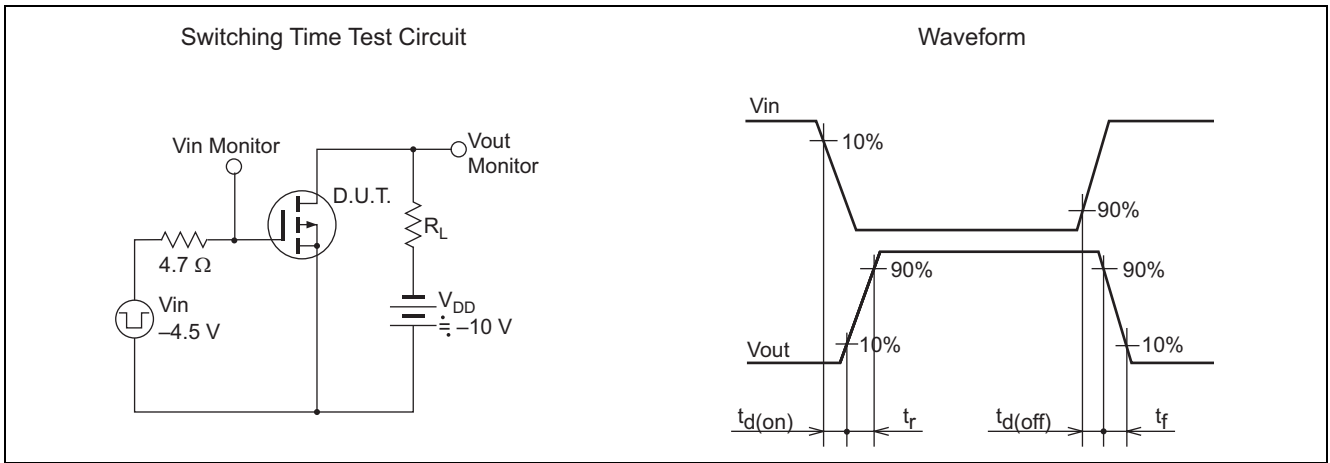
Drain to Source Saturation Voltage vs. Gate to Source Voltage



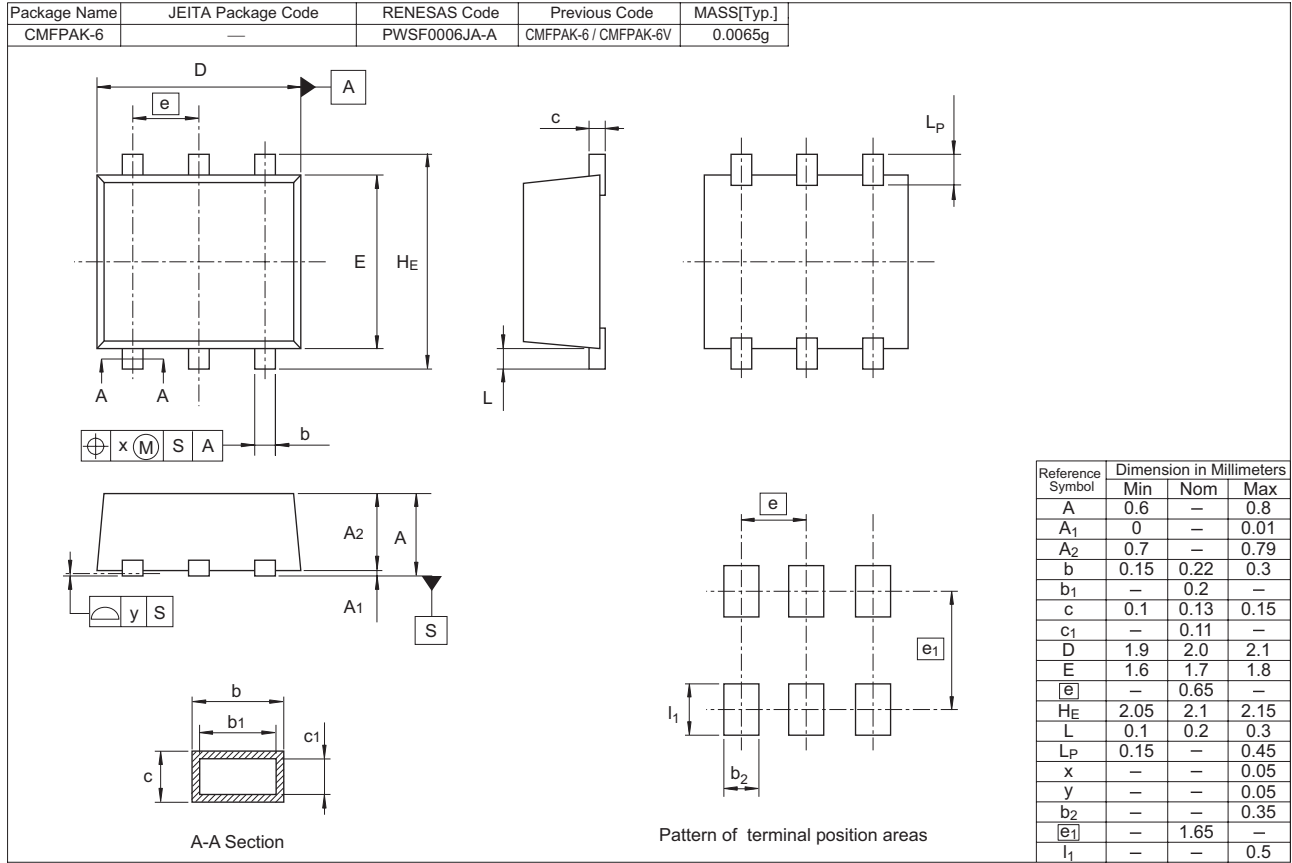
Static Drain to Source on State Resistance vs. Drain Current







Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAT1094C-EL-E	3000 pcs	Taping

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Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510