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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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HAT1044M

Silicon P Channel Power MOS FET Power Switching

REJ03G1152-0600

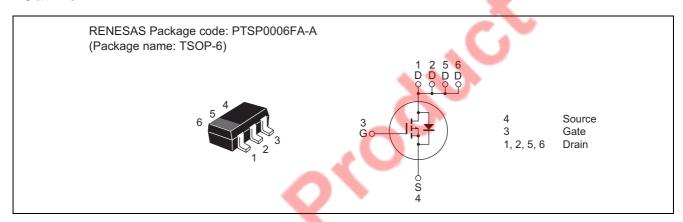
(Previous: ADE-208-753D)

Rev.6.00 Sep 07, 2005

Features

- Low on-resistance
- Low drive current
- High density mounting
- 4.5 V gate drive device can be driven from 5 V source

Outline



Absolute Maximum Ratings

 $(Ta = 25^{\circ}C)$

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-30	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D Note 2	-4.5	A
Drain peak current	I _{D (pulse)} Note 1	-18	A
Body-drain diode reverse drain current	I _{DR} Note 2	-4.5	А
Channel dissipation	Pch (pulse) Note 2	2.0	W
Channel dissipation	Pch (continuous) Note 3	1.05	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1. PW \leq 10 μ s, duty cycle \leq 1%

- 2. When using the alumina ceramic board (50 \times 50 \times 0.7 mm), PW \leq 5 s, Ta = 25 $^{\circ}C$
- 3. When using the alumina ceramic board ($50 \times 50 \times 0.7$ mm), Ta = 25° C

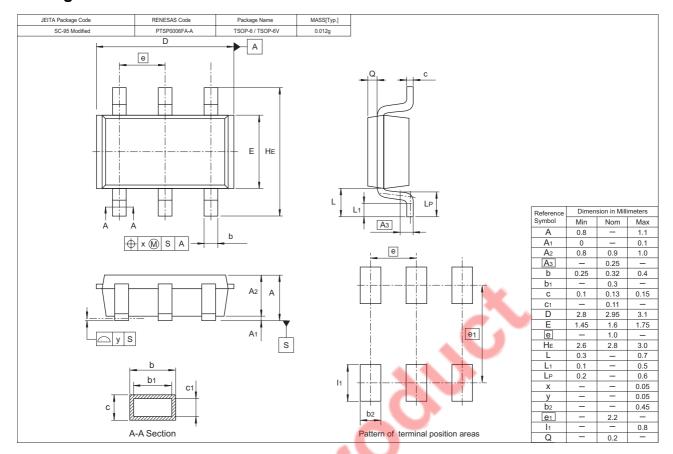
Electrical Characteristics

 $(Ta = 25^{\circ}C)$

Item	Symbol	Min	Тур	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-30	_		V	$I_D = -10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I _{GSS}		_	±0.1	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I _{DSS}		_	1	μΑ	$V_{DS} = -30 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	V _{GS (off)}	-1.0	4	-2.5	V	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$
Static drain to source on state resistance	R _{DS (on)}	_	50	60	mΩ	$I_D = -3 \text{ A}, V_{GS} = -10 \text{ V}^{\text{Note 4}}$
	R _{DS (on)}		80	105	mΩ	$I_D = -3 \text{ A}, V_{GS} = -4.5 \text{ V}^{\text{Note 4}}$
Forward transfer admittance	y _{fs}	3	5.5		S	$I_D = -3 \text{ A}, V_{DS} = -10 \text{ V}^{\text{Note 4}}$
Input capacitance	Ciss		600		pF	$V_{DS} = -10 \text{ V}$
Output capacitance	Coss	_	220		pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	_	150	_	pF	f = 1 MHz
Total gate charge	Qg	_	13	_	nC	V _{DS} = 10 V
Gate to source charge	Qgs	_	2	_	nC	$V_{GS} = 0$
Gate to drain charge	Qgd	_	3	_	nC	f = 1 MHz
Turn-on delay time	t _{d (on)}	_	12	_	ns	$V_{GS} = -10 \text{ V}, I_D = -3 \text{ A},$
Rise time	t _r	_	85	_	ns	$R_L = 3.3 \Omega$
Turn-off delay time	t _{d (off)}	_	55	_	ns	
Fall time	t _f	_	55	_	ns	
Body-drain diode forward voltage	V_{DF}	_	-0.95	_	V	$I_F = -4.5 \text{ A}, V_{GS} = 0$ Note 4
Body-drain diode reverse recovery time	t _{rr}	_	50	_	ns	$I_F = -4.5 \text{ A}, V_{GS} = 0$
						di _F /dt = -20 A/μs

Note: 4. Pulse test

Package Dimensions



Ordering Information

Part Name	Quantity	K	Shipping Container
HAT1044M-EL-E	3000 pcs		Taping

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Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
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Renesas Technology Korea Co., Ltd.Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd. Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia Tel: <603> 7955-9390, Fax: <603> 7955-9510

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