

## 30V N-Channel NexFET™ Power MOSFETs

Check for Samples: **CSD17559Q5**

### FEATURES

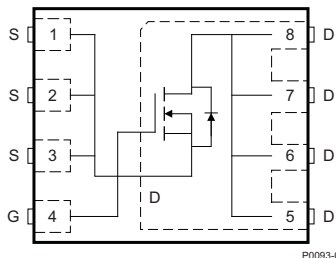
- Extremely Low Resistance
- Ultralow  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

### APPLICATIONS

- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems
- Synchronous Rectification
- Active ORing and Hotswap Applications

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in synchronous rectification and other power conversion applications.

**Top View**


P0093-01

### PRODUCT SUMMARY

$T_A = 25^\circ\text{C}$ unless otherwise stated		TYPICAL VALUE		UNIT
$V_{DS}$	Drain to Source Voltage	30		V
$Q_g$	Gate Charge Total (4.5V)	39		nC
$Q_{gd}$	Gate Charge Gate to Drain	9.3		nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5\text{V}$	1.15	m $\Omega$
		$V_{GS} = 10\text{V}$	0.95	m $\Omega$
$V_{GS(th)}$	Threshold Voltage	1.4		V

### ORDERING INFORMATION

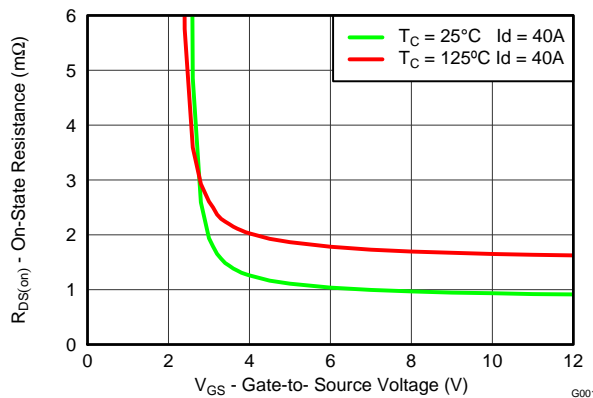
Device	Package	Media	Qty	Ship
CSD17559Q5	SON 5-mm x 6-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

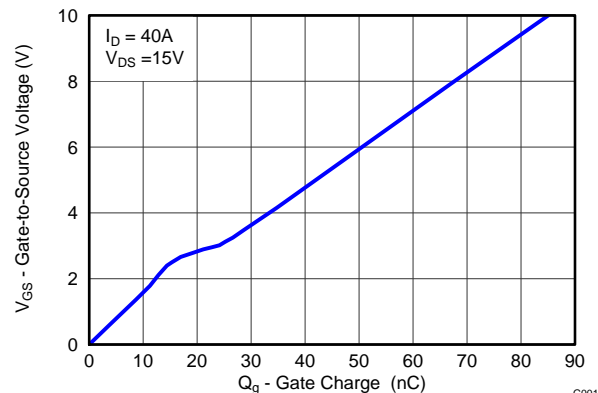
$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package limited), $T_C = 25^\circ\text{C}$	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	257	
	Continuous Drain Current <sup>(1)</sup>	40	
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(1)(2)</sup>	250	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.2	W
$T_J$ , $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 104\text{A}$ , $L = 0.1\text{mH}$ , $R_G = 25\Omega$	541	mJ

(1) Typical  $R_{\theta JA} = 40^\circ\text{C}/\text{W}$  on 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$

 **$R_{DS(on)}$  vs  $V_{GS}$** 


G001

**GATE CHARGE**


G001



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

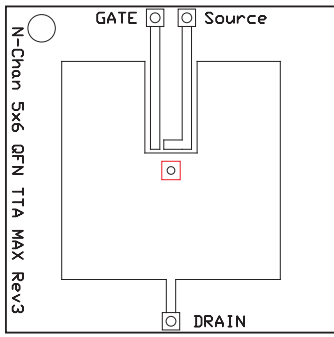
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain to Source Voltage	$V_{GS} = 0V, I_{DS} = 250\mu A$	30			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	$\mu A$
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = 20V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = 250\mu A$	1.2	1.4	1.7	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 4.5V, I_{DS} = 40A$		1.15	1.5	m $\Omega$
		$V_{GS} = 10V, I_{DS} = 40A$		0.95	1.15	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 15V, I_{DS} = 40A$		235		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V,$ $f = 1MHz$		7070	9200	pF
$C_{oss}$	Output Capacitance			1780	2314	pF
$C_{riss}$	Reverse Transfer Capacitance			87	113	pF
$R_G$	Series Gate Resistance			1.2	2.4	$\Omega$
$Q_g$	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_{DS} = 40A$		39	51	nC
$Q_{gd}$	Gate Charge Gate to Drain			9.3		nC
$Q_{gs}$	Gate Charge Gate to Source			14.4		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			8.3		nC
$Q_{oss}$	Output Charge	$V_{DS} = 15V, V_{GS} = 0V$		50		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V,$ $I_{DS} = 40A, R_G = 2\Omega$		20		ns
$t_r$	Rise Time			41		ns
$t_{d(off)}$	Turn Off Delay Time			32		ns
$t_f$	Fall Time			14		ns
<b>Diode Characteristics</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 40A, V_{GS} = 0V$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 15V, I_F = 40A, di/dt = 300A/\mu s$		80		nC
$t_{rr}$	Reverse Recovery Time			37		ns

## THERMAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

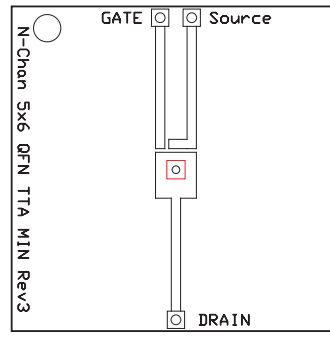
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1.2	$^\circ\text{C}/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)(2)</sup>			50	$^\circ\text{C}/W$

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch x 1.5-inch (3.81-cm x 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



M0137-01

Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of 2-  
oz. (0.071-mm thick)  
Cu.



M0137-02

Max  $R_{\theta JA} = 125^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

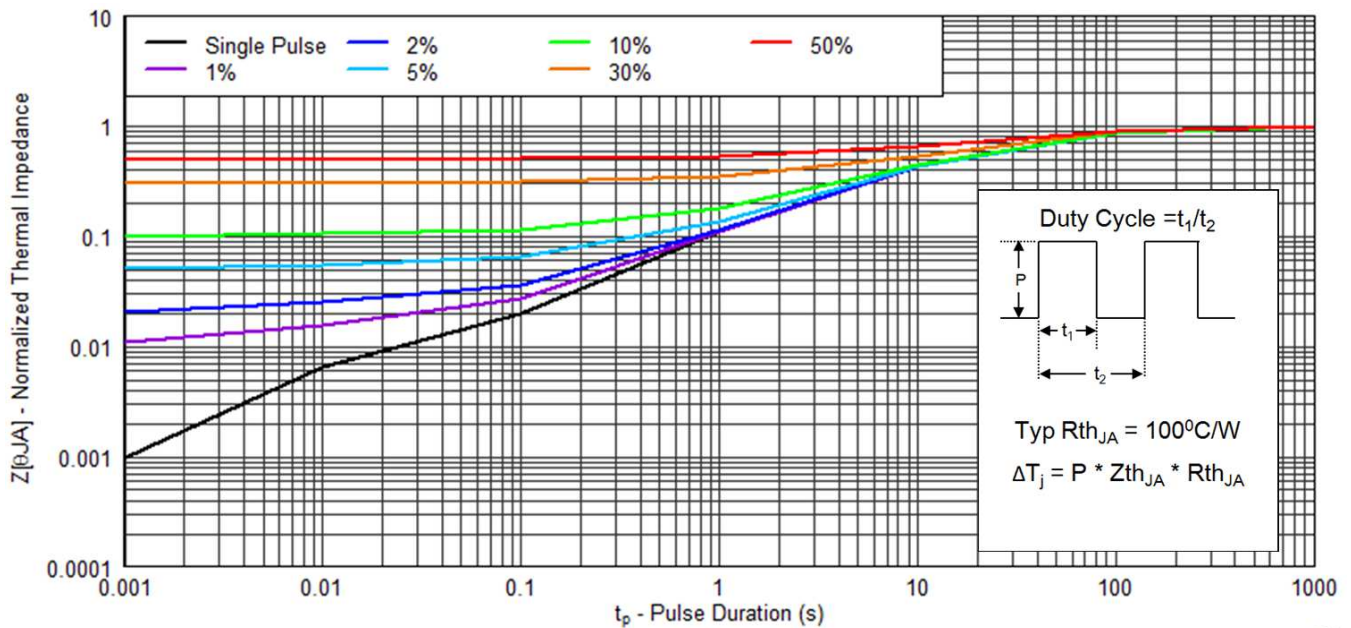
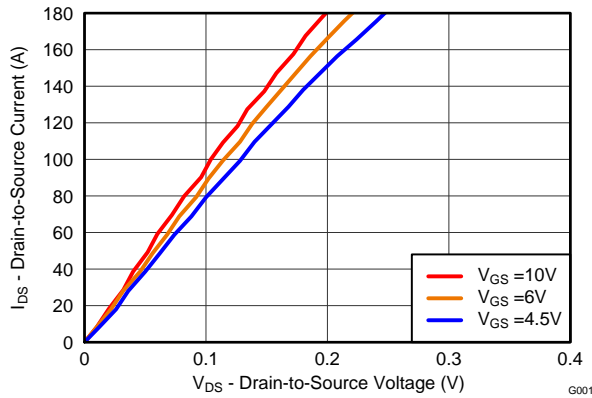


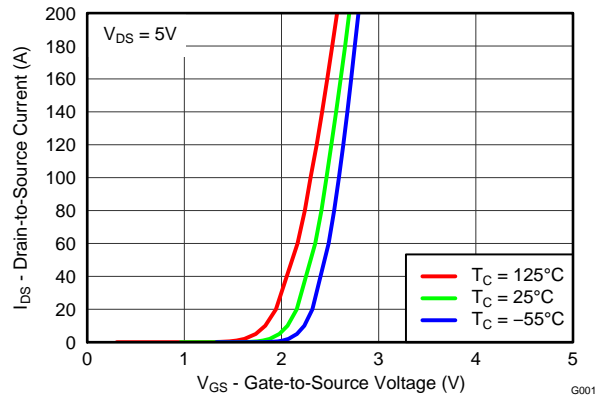
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

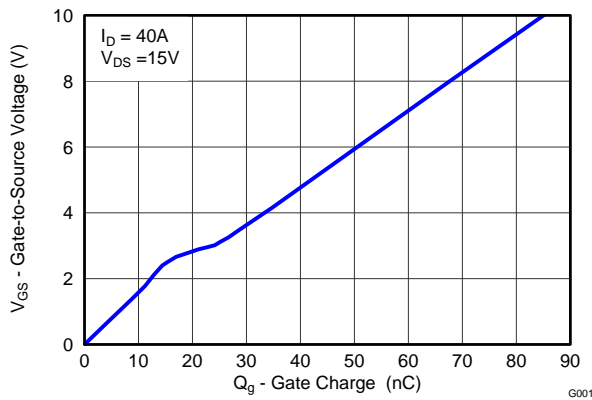
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



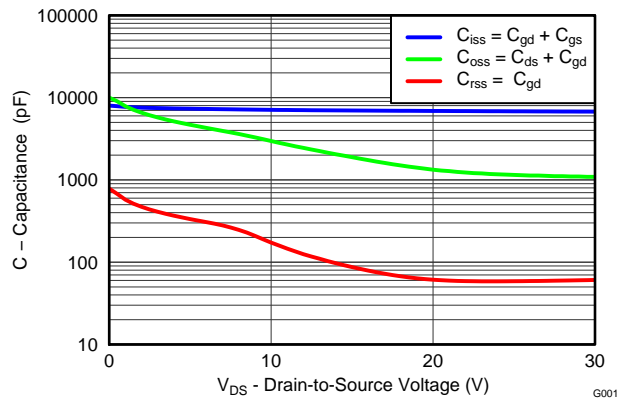
**Figure 2. Saturation Characteristics**



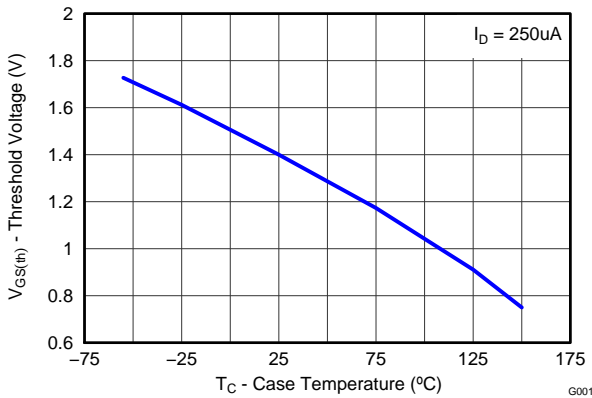
**Figure 3. Transfer Characteristics**



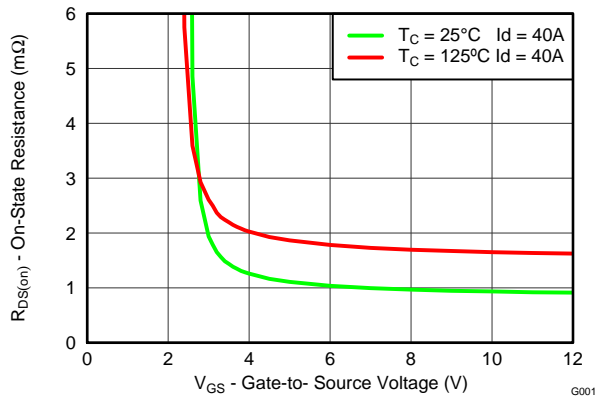
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

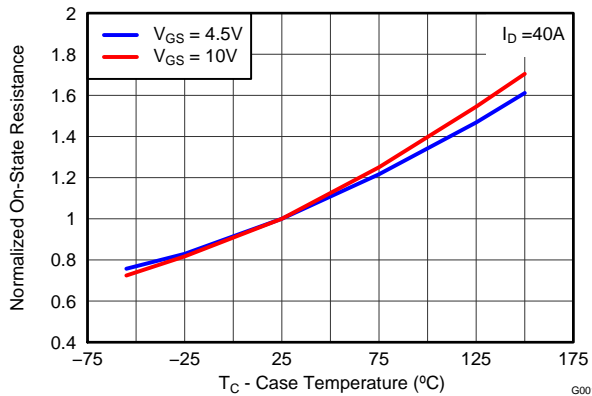


Figure 8. Normalized On-State Resistance vs. Temperature

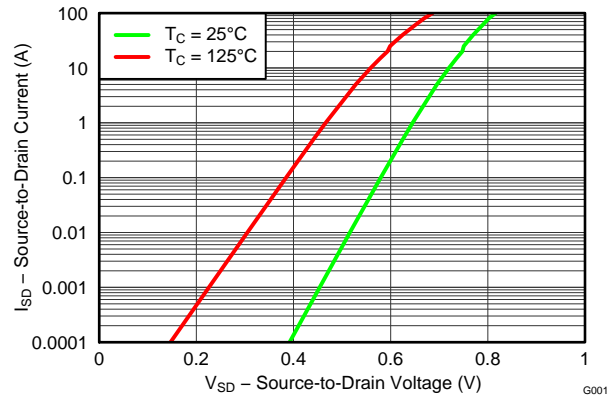


Figure 9. Typical Diode Forward Voltage

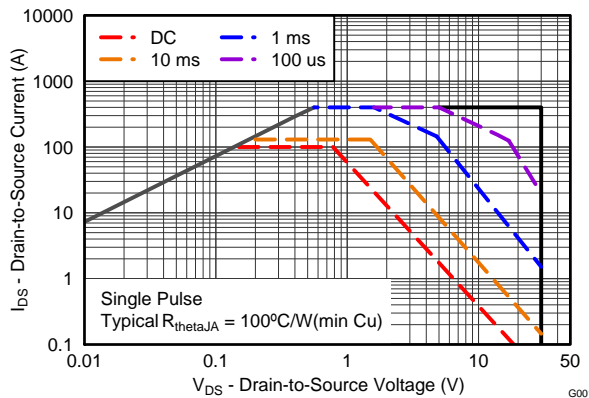


Figure 10. Safety Operating Area  $T_C = 25^\circ\text{C}$

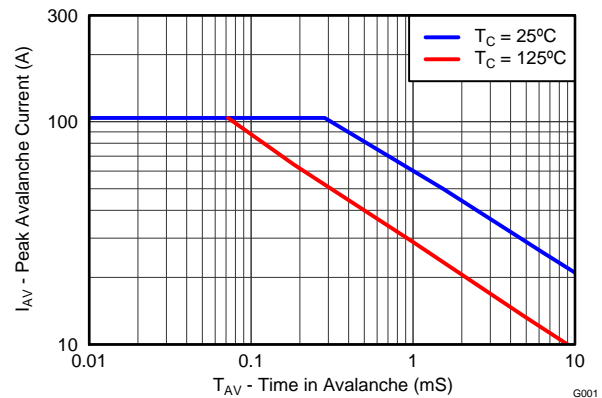


Figure 11. Single Pulse Unclamped Inductive Switching

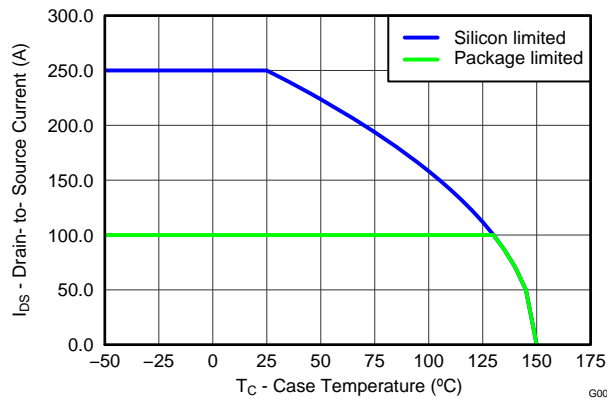
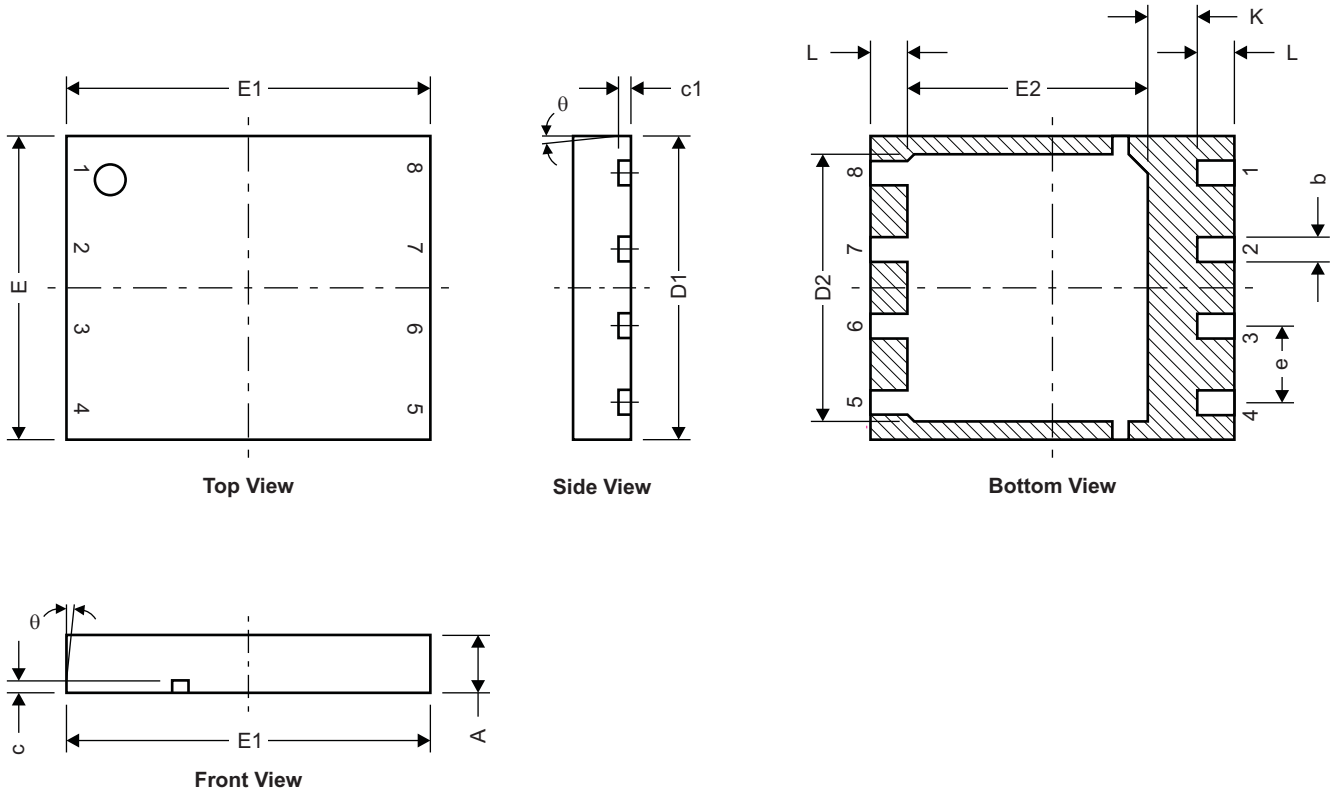


Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

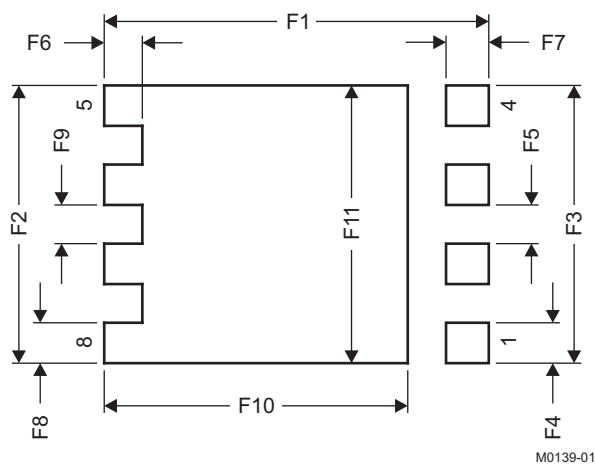
**Q5 Package Dimensions**



M0140-01

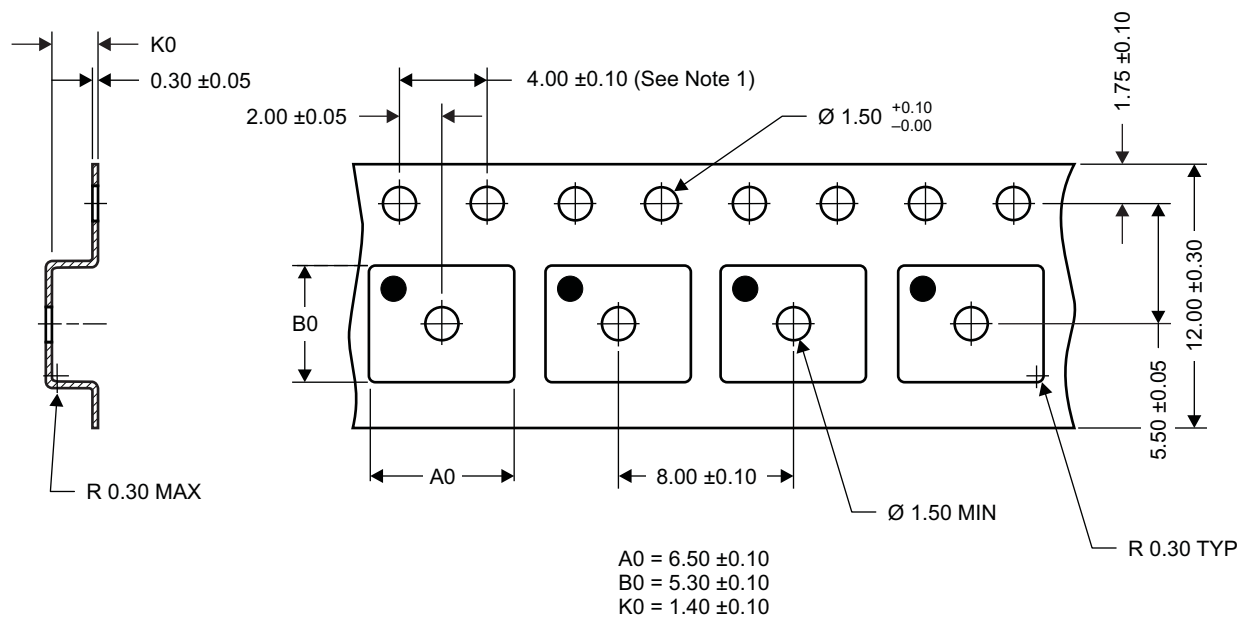
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.950	1.050	0.037	0.039
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
D1	4.900	5.100	0.193	0.201
D2	4.320	4.520	0.170	0.178
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.920	4.12	0.154	0.162
e	1.27 TYP		0.050	
K	0.760		0.030	
L	0.510	0.710	0.020	0.028
$\theta$	0.00			

Figure 13. Recommended PCB Pattern



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.460	4.560	0.176	0.180
F3	4.460	4.560	0.176	0.180
F4	0.650	0.700	0.026	0.028
F5	0.620	0.670	0.024	0.026
F6	0.630	0.680	0.025	0.027
F7	0.700	0.800	0.028	0.031
F8	0.650	0.700	0.026	0.028
F9	0.620	0.670	0.024	0.026
F10	4.900	5.000	0.193	0.197
F11	4.460	4.560	0.176	0.180

Q5 Tape and Reel Information



M0138-01

Notes:

1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm, unless otherwise specified.
5. Thickness:  $0.30 \pm 0.05$ mm
6. MSL1 260°C (IR and convection) PbF reflow compatible

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD17559Q5	SON	DQH	8	2500	330.0	12.8	6.5	5.3	1.4	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD17559Q5	SON	DQH	8	2500	335.0	335.0	32.0

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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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