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BUZ45A

N-Channel Enhancement-Mode Power Field-Effect Transistor

Features

- 8.3A, 500V
- $r_{DS(on)} = 0.8\Omega$
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

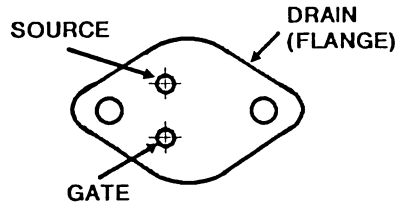
Description

The BUZ45A is an n-channel enhancement-mode silicon-gate power field-effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. This type can be operated directly from integrated circuits.

The BUZ45A is supplied in the JEDEC TO-204AA plastic package.

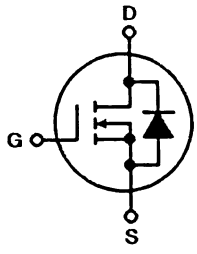
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		BUZ45A	UNITS
Drain-Source Voltage	V_{DS}	500	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	500	V
Continuous Drain Current T_C = +25°C	I_D	8.3	A
Pulsed Drain Current T_C = +25°C	I_{DM}	33	A
Gate-Source Voltage	V_{GS}	±20	V
Maximum Power Dissipation T_C = +25°C	P_D	125	W
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150	°C
DIN Humidity Category - DIN 40040		E	
IEC Climatic Category - DIN IEC 68-1		55/150/56	

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications BUZ45A

ELECTRICAL CHARACTERISTICS *At Case Temperature (T_C) = 25° C Unless Otherwise Specified*

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V I_D = 0.25 mA	500	—	—	V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} I_D = 1 mA	2.1	3	4	
Zero-Gate Voltage Drain Current	I_{DSS}	T_j = 25 °C T_j = 125 °C V_{DS} = 500 V, V_{GS} = 0 V	— —	20 100	250 1000	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 20 V V_{DS} = 0 V	—	10	100	nA
Drain-Source On Resistance	$r_{DS(on)}$	V_{GS} = 10 V I_D = 5 A	—	0.7	0.8	Ω
Forward Transconductance	g_{fs}	V_{DS} = 25 V I_D = 5 A	2.7	5	—	S
Input Capacitance	C_{iss}	V_{GS} = 0 V V_{DS} = 25 V f = 1 MHz	—	3800	4900	pF
Output Capacitance	C_{oss}		—	250	400	
Reverse Transfer Capacitance	C_{rss}		—	100	170	
Turn-On Time t_{on} (t_{on} = $t_{d(on)}$ + t_r)	$t_{d(on)}$ t_r	V_{CC} = 30 V I_D = 2.8 A V_{GS} = 10 V R_{GS} = 50 Ω	— —	50 80	75 120	ns
Turn-Off Time t_{off} (t_{off} = $t_{d(off)}$ + t_r)	$t_{d(off)}$ t_r		— —	330 110	430 140	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		≤ 1			°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$		≤ 35			

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Continuous Reverse Drain Current	I_{DR}	T_C = 25 °C	—	—	8.3	A
Pulsed Reverse Drain Current	I_{DRM}		—	—	33	
Diode Forward Voltage	V_{SD}	I_F = 2 x I_{DR} V_{GS} = 0 V, T_j = 25 °C	—	1.3	1.6	V
Reverse Recovery Time	t_{rr}	T_j = 25°C, I_F = I_{DR}	—	1200	—	ns
Reverse Recovered Charge	Q_{RR}	dI_F/dt = 100 A/μs, V_R = 100 V	—	12	—	μC

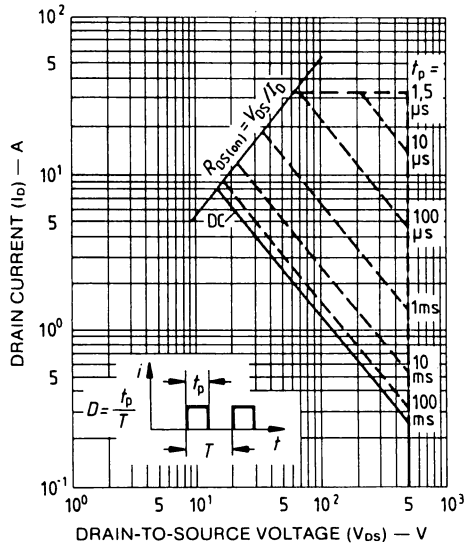


Fig. 1 - Maximum safe operating areas for all types.

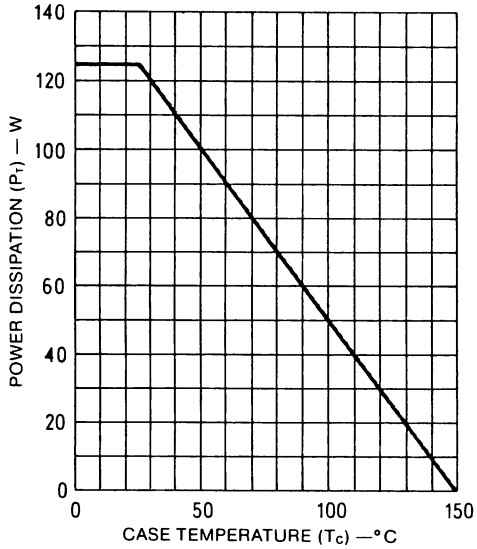


Fig. 2 - Power vs. temperature derating curve for all types.

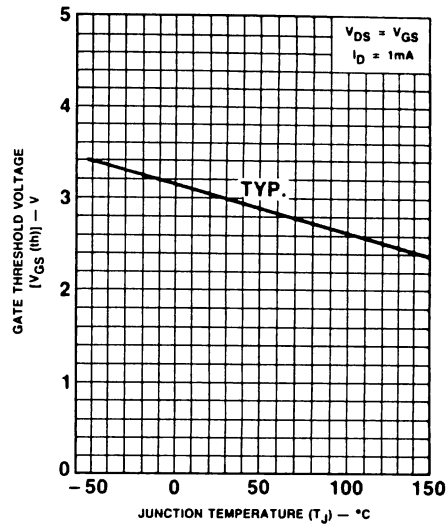


Fig. 3 - Normalized gate threshold voltage as a function of junction temperature for all types.

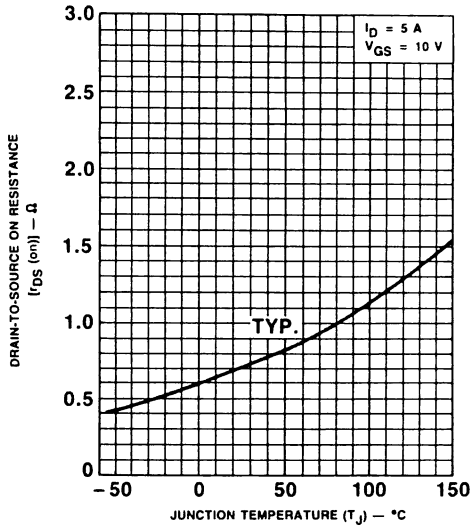


Fig. 4 - Normalized drain-to-source on resistance to junction temperature for all types.

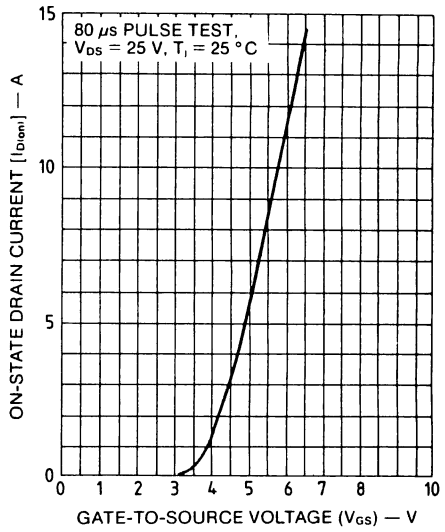


Fig. 5 - Typical transfer characteristics for all types.

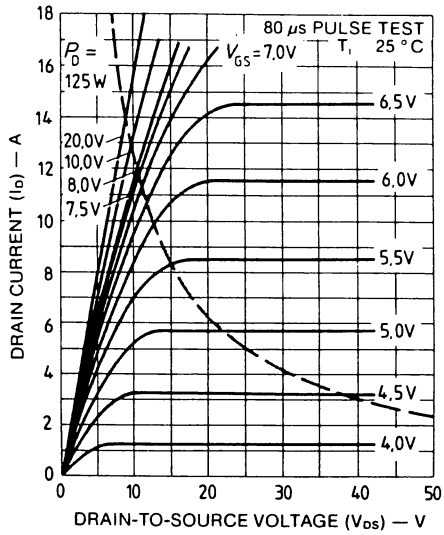


Fig. 6 - Typical output characteristics.

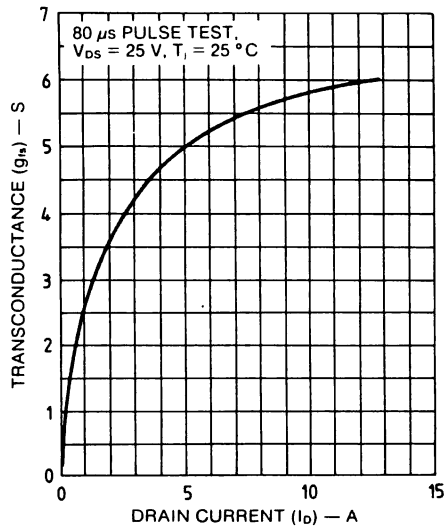


Fig. 7 - Typical transconductance vs. drain current.

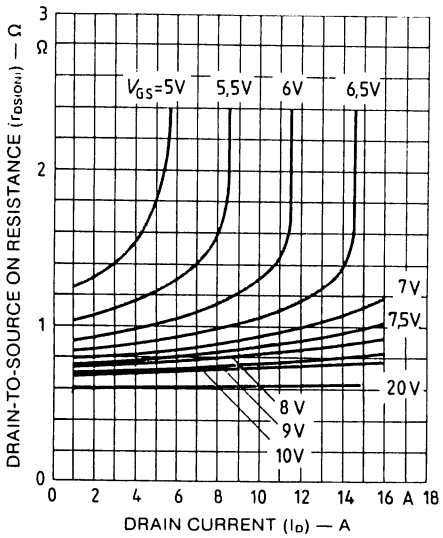


Fig. 8 - Typical on-resistance vs. drain current.

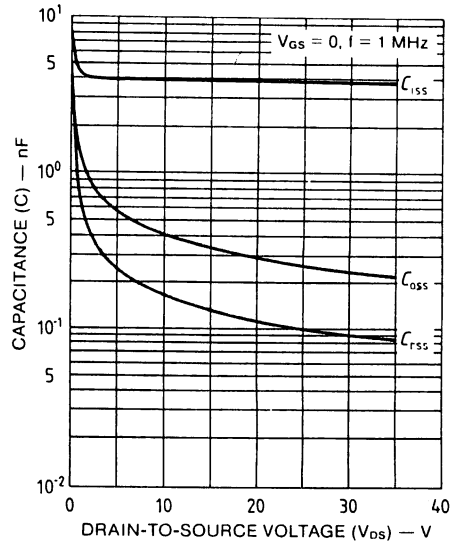


Fig. 9 - Typical capacitance vs. drain-to-source voltage.

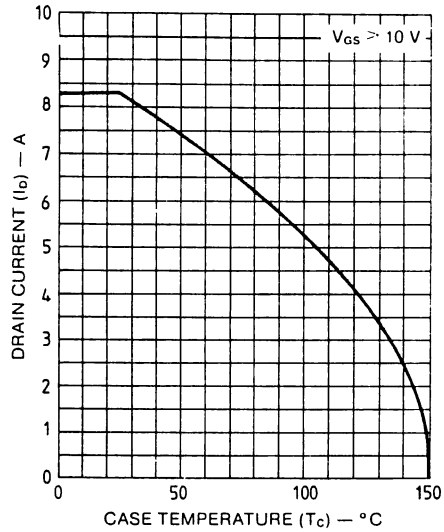


Fig. 10 - Maximum drain current vs. case temperature.

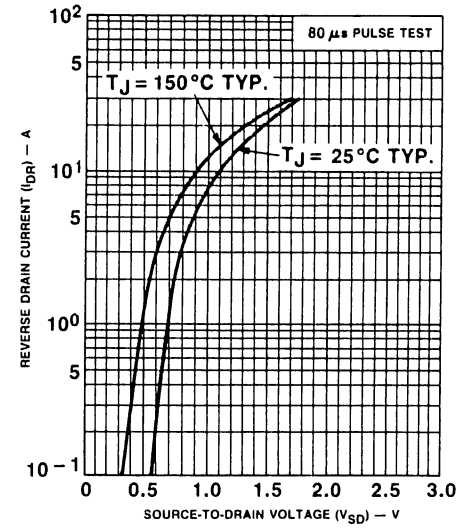


Fig. 11 - Typical source-drain diode forward voltage.

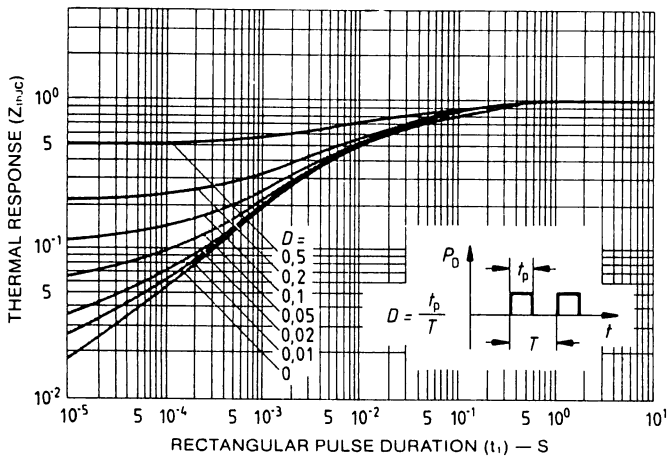


Fig. 12 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

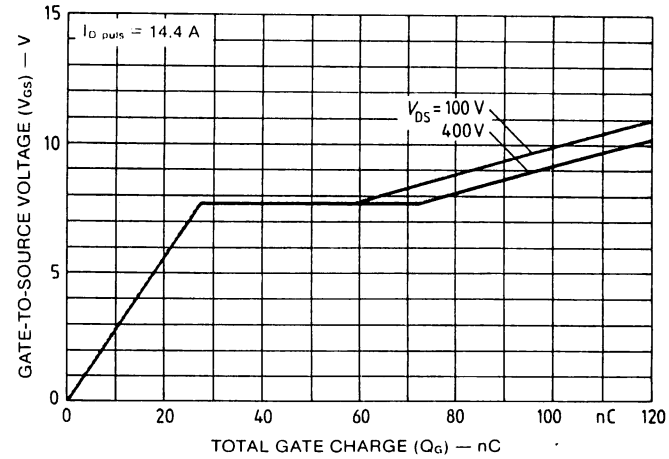
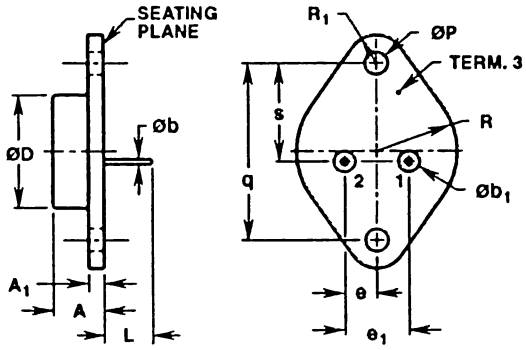


Fig. 13 - Typical gate charge vs. gate-to-source voltage.

Hermetic Steel Packages



NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-204AA outline dated 11-82.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of seating plane.
5. Controlling dimension: Inch.
6. Revision 2 dated 6-93.

TO-204AA

JEDEC TO-204AA HERMETIC STEEL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.310	0.330	7.88	8.38	-
A_1	0.060	0.065	1.53	1.65	-
Øb	0.038	0.042	0.97	1.06	2, 3
$Øb_1$	0.138	0.145	3.51	3.68	-
ØD	-	0.800	-	20.32	-
e	0.215 TYP		5.46 TYP		4
e_1	0.430 BSC		10.92 BSC		4
L	0.430	-	10.93	-	-
ØP	0.155	0.160	3.94	4.06	-
q	1.187 BSC		30.15 BSC		-
R	0.495	0.525	12.58	13.33	-
R_1	0.131	0.185	3.33	4.69	-
s	0.655	0.675	16.64	17.14	-