

Surface Mount Dual N-Channel Enhancement Mode MOSFET

(Pb) Lead(Pb)-Free

Features:

*Super high dense cell design for low R_{DS(ON)}

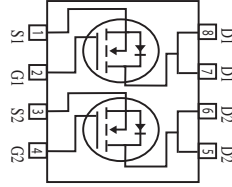
$$R_{DS(ON)} < 50m\Omega \text{ @ } V_{GS} = 10V$$

$$R_{DS(ON)} < 60m\Omega \text{ @ } V_{GS} = 4.5V$$

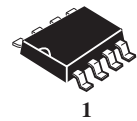
*Simple Drive Requirement

*Dual N MOSFET Package

*SO-8 Package



DRAIN CURRENT
5 AMPERES
DRAIN SOURCE VOLTAGE
60 VOLTAGE



1

SO-8

Maximum Ratings (TA=25°C Unless Otherwise Specified)

Rating	Symbol	Value	Unite
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current ⁽¹⁾ (T _A = 25°C) (T _A = 70°C)	I _D	5.0	A
		3.2	A
Pulsed Drain Current ⁽²⁾	I _{DM}	30	A
Power Dissipation ⁽¹⁾ (T _A = 25°C)	P _D	2	W
Maximax Junction-to-Ambient ⁽¹⁾	R _{θJA}	62.5	°C/W
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

Device Marking

WTK9971=9971SS

Electrical Characteristics (T_A=25 °C Unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	60	-	-	V	V _{GS} =0, I _D =250uA
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _j	-	0.06	-	V/°C	Reference to 25°C, I _D =1mA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D =250uA
Forward Transconductance	g _{fs}	-	7	-	S	V _{DS} =10V, I _D =5A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±25V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	1	uA	V _{DS} =60V, V _{GS} =0
Drain-Source Leakage Current(T _j =70°C)		-	-	25	uA	V _{DS} =48V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	-	50	mfl	V _{GS} =10V, I _D =5A
		-	-	60		V _{GS} =4.5V, I _D =2.5A
Total Gate Charge ²	Q _g	-	32.5	-	nC	I _D =5A V _{DS} =48V V _{GS} =10V
Gate-Source Charge	Q _{gs}	-	4.9	-		
Gate-Drain ("Miller") Charge	Q _{gd}	-	8.8	-		
Turn-on Delay Time ²	T _{d(on)}	-	9.6	-	ns	V _{DS} =30V I _D =5A V _{GS} =10V R _G =3.3fl R _D =6fl
Rise Time	T _r	-	10	-		
Turn-off Delay Time	T _{d(off)}	-	30	-		
Fall Time	T _f	-	5.5	-		
Input Capacitance	C _{iss}	-	1658	-	pF	V _{GS} =0V V _{DS} =25V f=1.0MHz
Output Capacitance	C _{oss}	-	156	-		
Reverse Transfer Capacitance	C _{rss}	-	109	-		

Source-Drain Diode

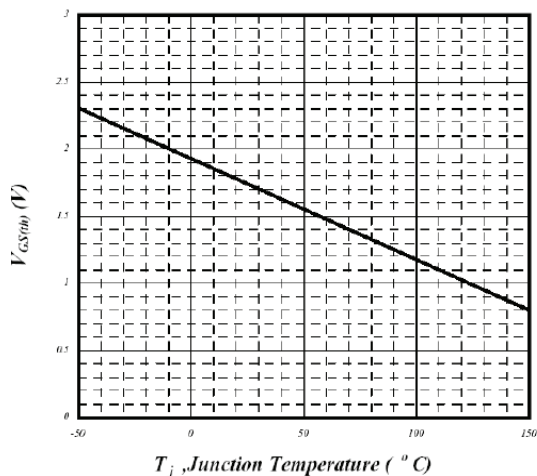
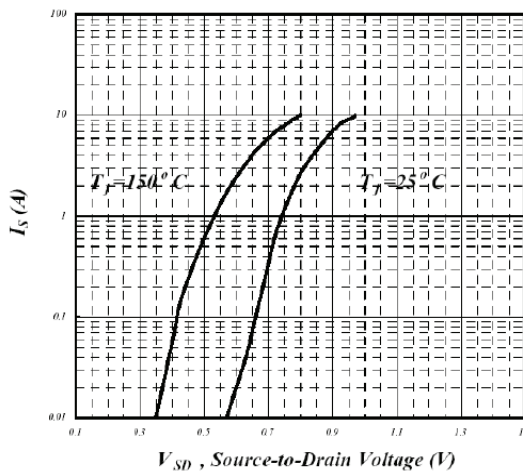
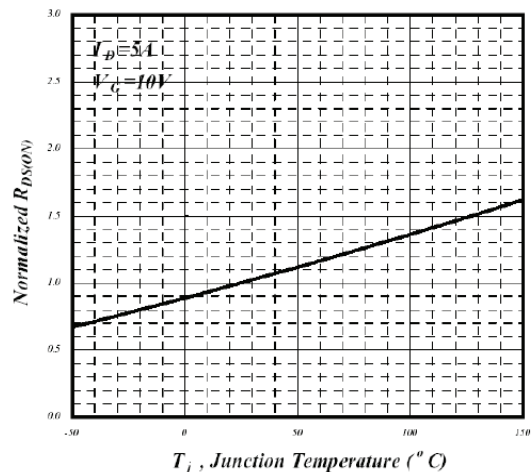
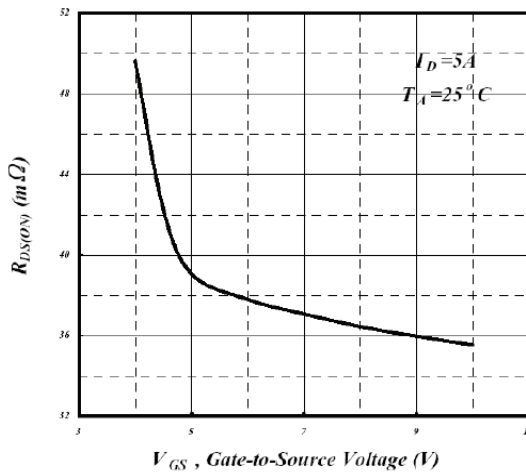
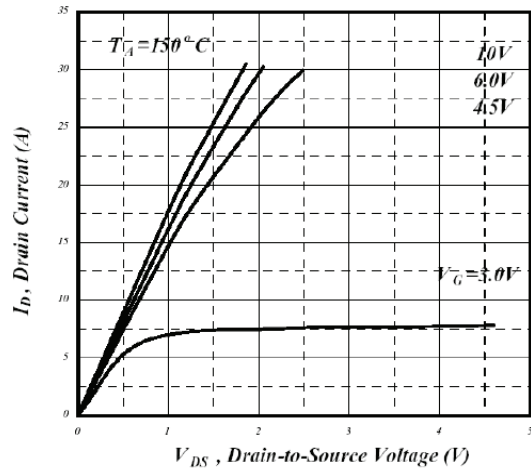
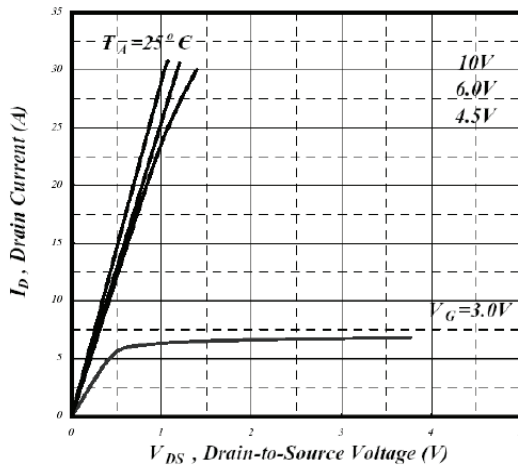
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	1.2	V	I _S =1.6A, V _{GS} =0V
Reverse Recovery Time	T _{rr}	-	29.2	-	ns	I _S =5A, V _{GS} =0V di/dt=100A/?s
Reverse Recovery Charge	Q _{rr}	-	48	-	nC	

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Surface mounted on 1 in² copper pad of FR4 board; 135°C/W when mounted on Min. copper pad.

Characteristics Curve



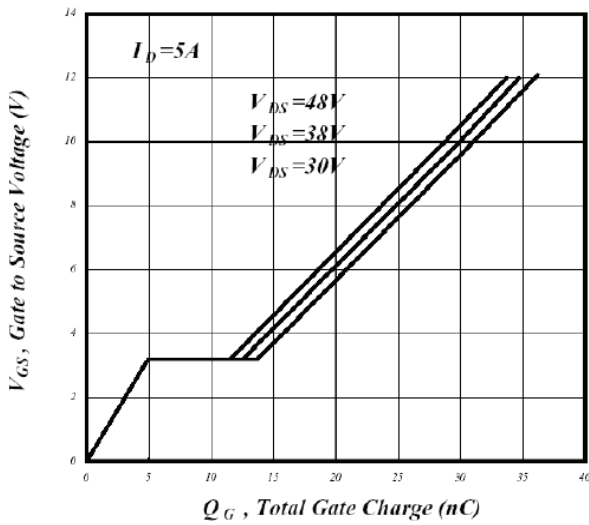


Fig 7. Gate Charge Characteristics

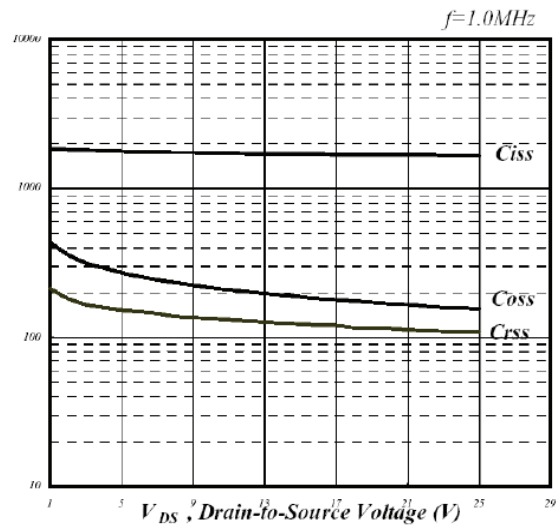


Fig 8. Typical Capacitance Characteristics

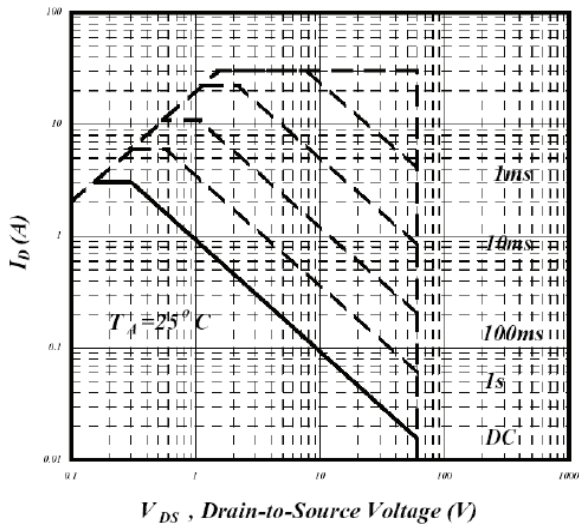


Fig 9. Maximum Safe Operating Area

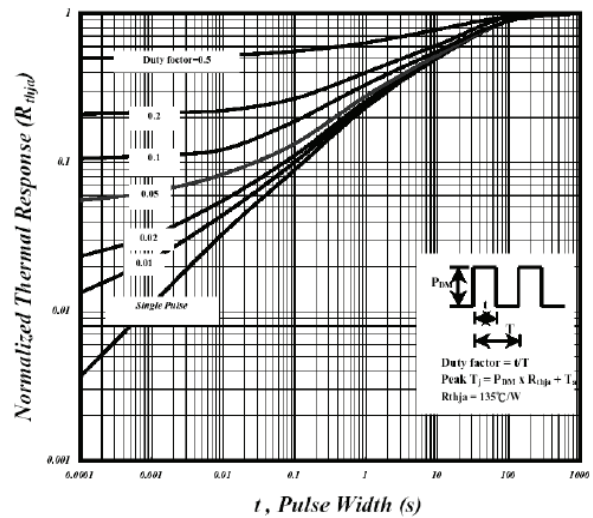


Fig 10. Effective Transient Thermal Impedance

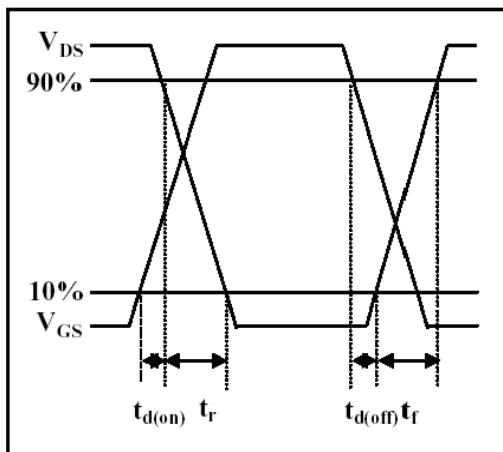


Fig 11. Switching Time Waveform

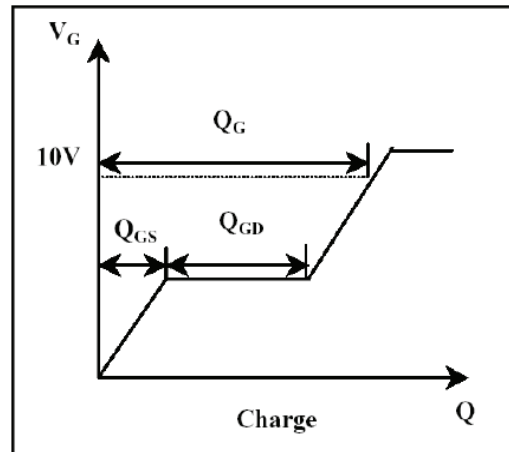
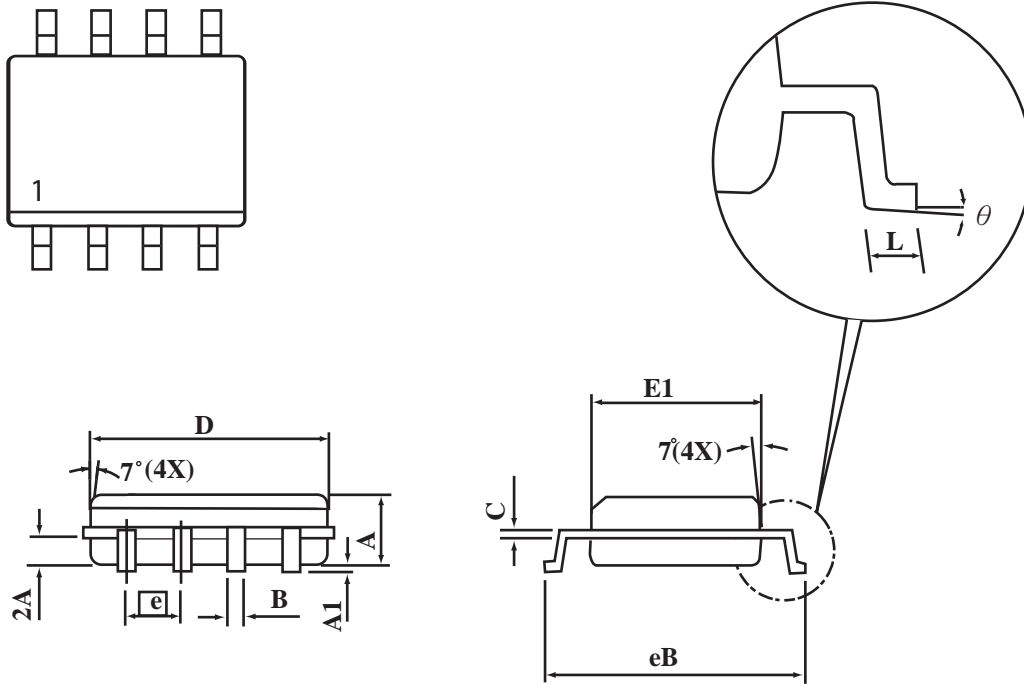


Fig 12. Gate Charge Waveform

SO-8 Package Outline Dimensions

Unit:mm



SYMBOLS	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.20
B	0.35	0.45
C	0.18	0.23
D	4.69	4.98
E1	3.56	4.06
eB	5.70	6.30
e	1.27 BSC	
L	0.60	0.80
θ	0°	8°