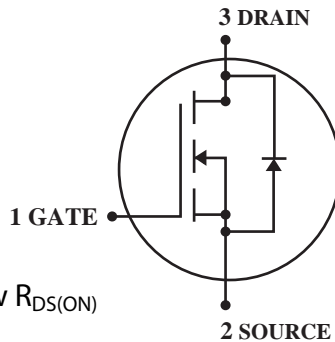


N-Channel Enhancement Mode Power MOSFET

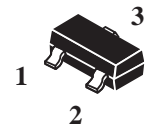
(Pb) Lead(Pb)-Free



DRAIN CURRENT
4.9 AMPERES
DRAIN SOURCE VOLTAGE
20 VOLTAGE

Features:

- * Super High Dense Cell Design For Low $R_{DS(ON)}$
 $R_{DS(ON)} < 41m\Omega$ @ $V_{GS}=4.5V$
 $R_{DS(ON)} < 47m\Omega$ @ $V_{GS}=2.5V$
 $R_{DS(ON)} < 57m\Omega$ @ $V_{GS}=1.8V$
- * Capable of 2.5V gate drive
- * Rugged and Reliable
- * Lower On-Resistance



SOT-23

Application:

- * Power Management in Notebook Computer.
- * Portable Equipment.
- * Battery Powered System.

Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Specified)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ³ , $V_{GS}@4.5V(T_A=25^\circ C)$ $V_{GS}@4.5V(T_A=70^\circ C)$	I_D	4.9	A
		3.4	
Pulsed Drain Current ^{1,2}	I_{DM}	15	
Total Power Dissipation($T_A=25^\circ C$)	P_D	0.75	W
Maximum Junction-ambient ³	$R_{\theta JA}$	140	$^\circ C/W$
Operating Junction Temperature Range	T_J	+150	$^\circ C$
Storage Temperature Range	T_{stg}	-55~+150	$^\circ C$

Device Marking

WTC2312=N12

Electrical Characteristics ($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Static

Drain-Source Breakdown Voltage $V_{GS}=0, I_D=250\mu\text{A}$	$V_{(BR)DSS}$	20	-	-	V
Gate-Source Threshold Voltage $V_{DS}=V_{GS}, I_D=250\mu\text{A}$	$V_{GS(Th)}$	0.4	0.6	1.0	
Gate-Source Leakage Current $V_{GS}=\pm 8\text{V}$	I_{GSS}	-	-	± 100	nA
Drain-Source Leakage Current ($T_j=25^{\circ}\text{C}$) $V_{DS}=20\text{V}, V_{GS}=0$	I_{DSS}	-	-	1	μA
Drain-Source On-Resistance $V_{GS}=1.8\text{V}, I_D=4.0\text{A}$ $V_{GS}=2.5\text{V}, I_D=4.5\text{A}$ $V_{GS}=4.5\text{V}, I_D=5.0\text{A}$	$R_{DS(on)}$	-	31 24 21	57 47 41	$\text{m}\Omega$
Forward Transconductance $V_{DS}=10\text{V}, I_D=5.0\text{A}$	g_{fs}	-	40	-	

Dynamic

Input Capacitance $V_{GS}=0\text{V}, V_{DS}=8\text{V}, f=1.0\text{MHz}$	C_{iss}	-	500	-	μF
Output Capacitance $V_{GS}=0\text{V}, V_{DS}=8\text{V}, f=1.0\text{MHz}$	C_{oss}	-	300	-	
Reverse Transfer Capacitance $V_{GS}=0\text{V}, V_{DS}=8\text{V}, f=1.0\text{MHz}$	C_{rss}	-	140	-	

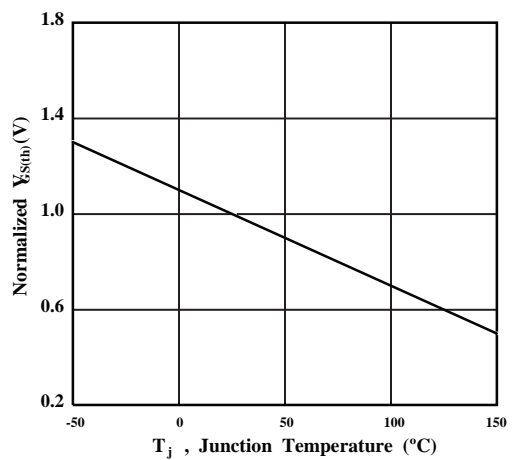
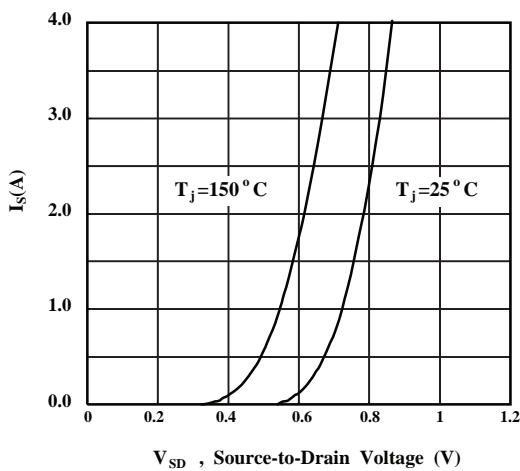
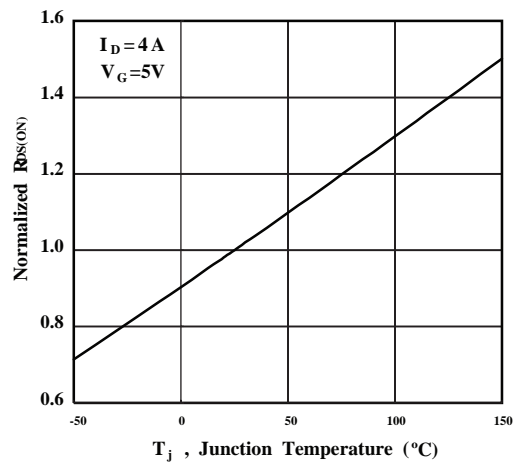
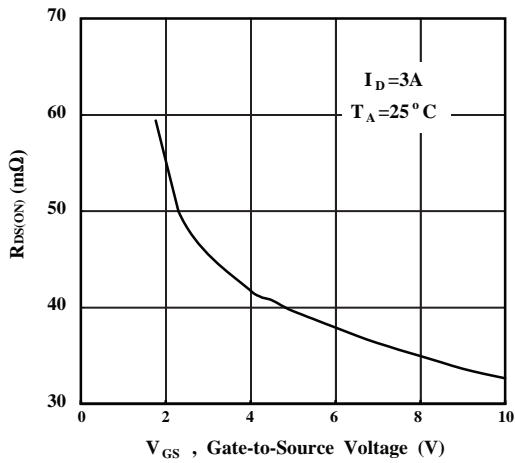
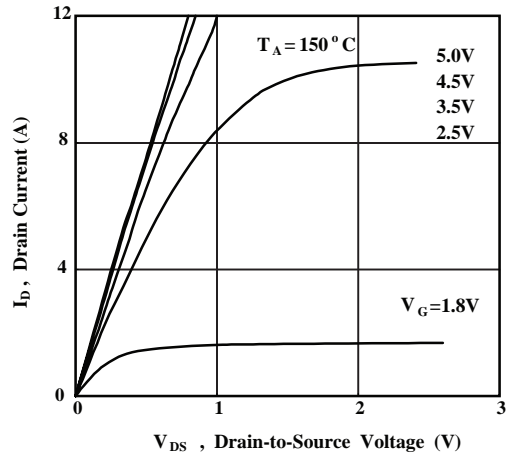
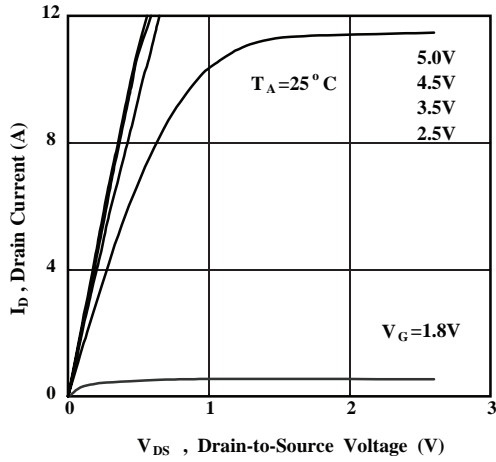
Switching

Turn-on Delay Time ² $V_{GEN}=4.5V, V_{DD}=10V, I_D=1.0A, R_G=6\Omega$	$t_{d(on)}$	-	15	25	ns
Rise Time $V_{GEN}=4.5V, V_{DD}=10V, I_D=1.0A, R_G=6\Omega$	t_r	-	40	60	
Turn-off Delay Time $V_{GEN}=4.5V, V_{DD}=10V, I_D=1.0A, R_G=6\Omega$	$t_{d(off)}$	-	48	70	
Fall Time $V_{GEN}=4.5V, V_{DD}=10V, I_D=1.0A, R_G=6\Omega$	t_f	-	31	45	
Total Gate Charge ² $V_{DS}=10V, V_{GS}=4.5V, I_D=5A$	Q_g	-	11.2	-	nC
Gate-Source Charge $V_{DS}=10V, V_{GS}=4.5V, I_D=5A$	Q_{gs}	-	1.4	-	
Gate-Drain Change $V_{DS}=10V, V_{GS}=4.5V, I_D=5A$	Q_{gd}	-	2.2	-	

Source-Drain Diode Characteristics

Forward On Voltage ² $V_{GS}=0V, I_S=1.7A$	V_{SD}	-	-	1.2	V
Diode Forward Current	I_S	-	-	1.7	A

- Note: 1. Pulse width limited by Max, junction temperature.
 2. pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 3. Surface mounted on 1 in² copper pad of PCB board.



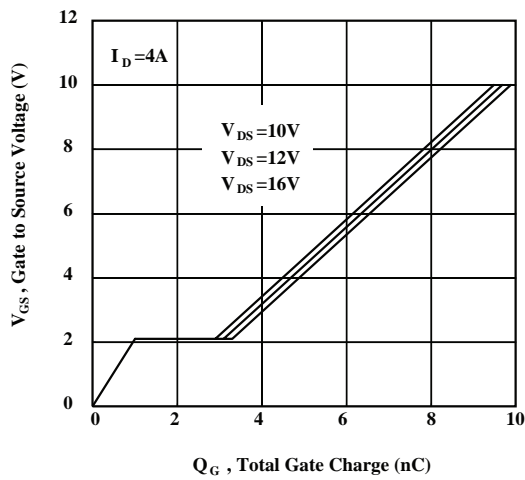


Fig 7. Gate Charge Characteristics

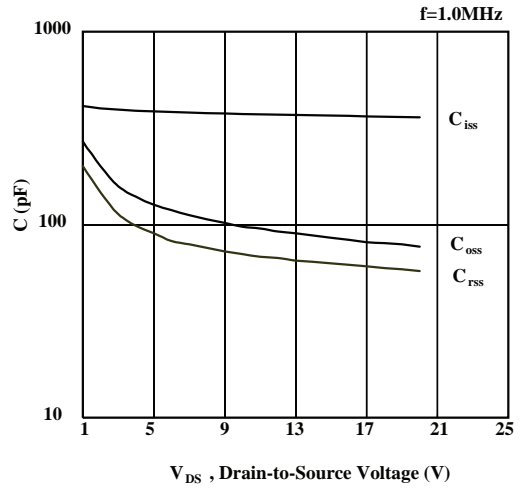


Fig 8. Typical Capacitance Characteristics

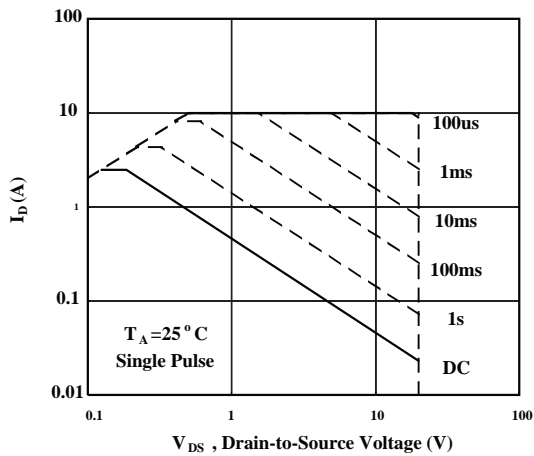


Fig 9. Maximum Safe Operating Area

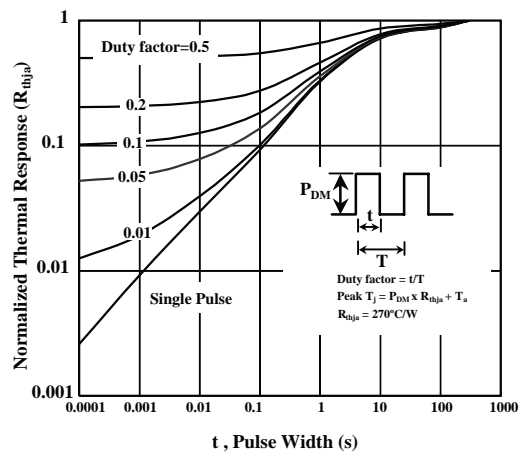


Fig 10. Effective Transient Thermal Impedance

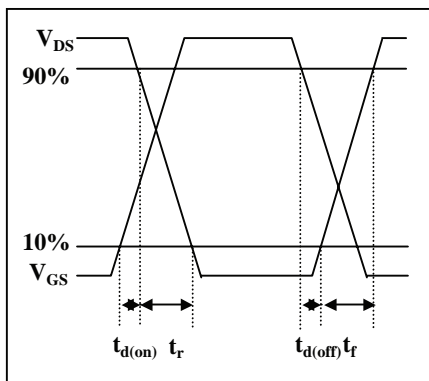


Fig 11. Switching Time Circuit

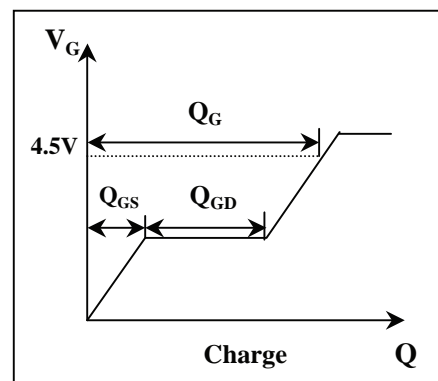
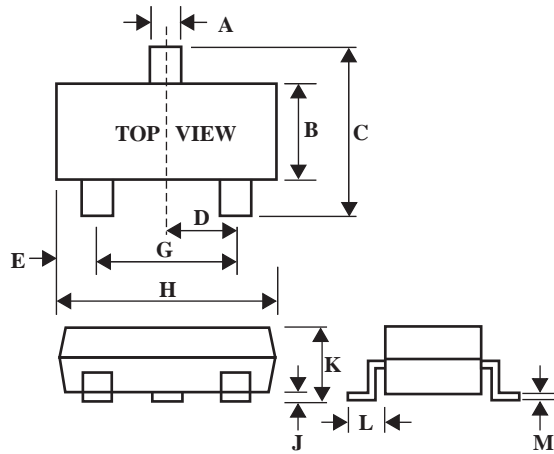


Fig 12. Gate Charge Circuit

SOT-23 Outline Dimension



SOT-23		
Dim	Min	Max
A	0.35	0.51
B	1.19	1.40
C	2.10	3.00
D	0.85	1.05
E	0.46	1.00
G	1.70	2.10
H	2.70	3.10
J	0.01	0.13
K	0.89	1.10
L	0.30	0.61
M	0.076	0.25