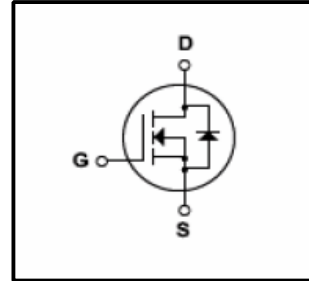


Silicon N-Channel MOSFET

Features

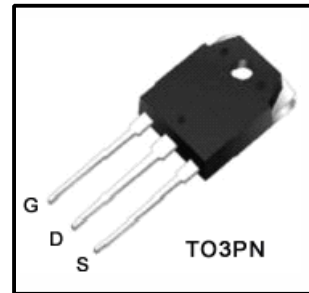
- 9A,900V, $R_{DS(on)}$ (Max1.35 Ω)@ $V_{GS}=10V$
- Ultra-low Gate charge(Typical 58nC)
- Fast Switching Capability
- 100%Avalanche Tested
- Maximum Junction Temperature Range(150 °C)



General Description

These N-Channel enhancement mode power field effect transistors are produced using Winsemi's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.



Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{DSS}	Drain Source Voltage	900	V
I_D	Continuous Drain Current(@ $T_c=25^\circ C$)	9	A
	Continuous Drain Current(@ $T_c=100^\circ C$)	5.7	A
I_{DM}	Drain Current Pulsed (Note1)	27	A
V_{GS}	Gate to Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note2)	663	mJ
E_{AR}	Repetitive Avalanche Energy (Note1)	15	mJ
dv/dt	Peak Diode Recovery dv /dt (Note3)	4.5	V/ ns
P_D	Total Power Dissipation(@ $T_c=25^\circ C$)	150	W
T_J, T_{stg}	Junction and Storage Temperature	-55~150	$^\circ C$
T_L	Channel Temperature	300	$^\circ C$

Thermal Characteristics

Symbol	Parameter	Value			Units
		Min	Typ	Max	
R_{QJC}	Thermal Resistance , Junction -to -Case	-	-	0.83	$^\circ C/W$
R_{QJA}	Thermal Resistance , Junction-to -Ambient	-	-	50	$^\circ C/W$

Electrical Characteristics(Tc=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit	
Gate leakage current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	-	±10	nA	
Gate-source breakdown voltage	V _{(BR)GSS}	I _G =±10 μA, V _{DS} =0V	±30	-	-	V	
Drain cut -off current	I _{DSS}	V _{DS} =720V, V _{GS} =0V	-	-	100	μA	
Drain -source breakdown voltage	V _{(BR)DSS}	I _D =10 mA, V _{GS} =0V	900	-	-	V	
Gate threshold voltage	V _{GS(th)}	V _{DS} =10V, I _D =1mA	3	-	5	V	
Drain -source ON resistance	R _{DS(ON)}	V _{GS} =10V, I _D =4A	-	1.1	1.35	Ω	
Forward Transconductance	g _{fs}	V _{DS} =15V, I _D =4A	3.0	7.0	-	S	
Input capacitance	C _{iss}	V _{DS} =25V,	-	2040	-	pF	
Reverse transfer capacitance	C _{rss}	V _{GS} =0V,	-	45	-		
Output capacitance	C _{oss}	f=1MHz	-	190	-		
Switching time	Rise time	t _r	V _{DD} =400V, I _D =4A R _G =100Ω (Note4,5)	-	25	-	ns
	Turn-on time	t _{on}		-	60	-	
	Fall time	t _f		-	20	-	
	Turn-off time	t _{off}		-	95	-	
Total gate charge(gate-source plus gate-drain)	Q _g	V _{DD} =400V, V _{GS} =10V,	-	58	-	nC	
Gate-source charge	Q _{gs}	I _D =9A	-	32	-		
Gate-drain("miller") Charge	Q _{gd}	(Note4,5)	-	26	-		

Source-Drain Ratings and Characteristics(Ta=25°C)

Characteristics	Symbol	Test Condition	Min	Type	Max	Unit
Continuous drain reverse current	I _{DR}	-	-	-	9	A
Pulse drain reverse current	I _{DRP}	-	-	-	27	A
Forward voltage(diode)	V _{DSF}	I _{DR} =9A, V _{GS} =0V	-	-	1.4	V
Reverse recovery time	t _{rr}	I _{DR} =9A, V _{GS} =0V,	-	1.6	-	ns
Reverse recovery charge	Q _{rr}	dI _{DR} / dt =100 A / μs	-	20	-	μC

Note 1.Repeativity rating :pulse width limited by junction temperature

2.L=15mH I_{AS}=9A, V_{DD}=90V, R_G=25Ω, Starting T_J=25°C

3.I_{SD}≤9A, di/dt≤200A/us, V_{DD}<BV_{DSS}, STARTING T_J=25°C

4.Pulse Test:Pulse Width≤300us, Duty Cycle≤2%

5. Essentially independent of operating temperature.

This transistor is an electrostatic sensitive device

Please handle with caution

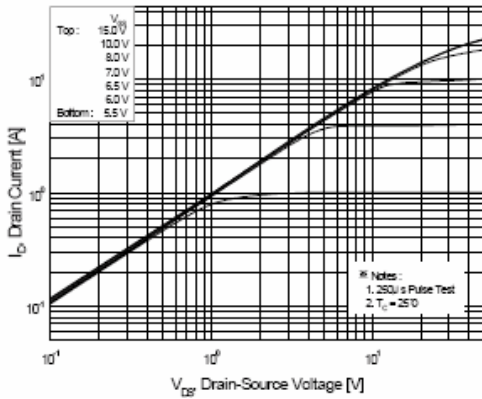


Fig.1 On State Characteristics

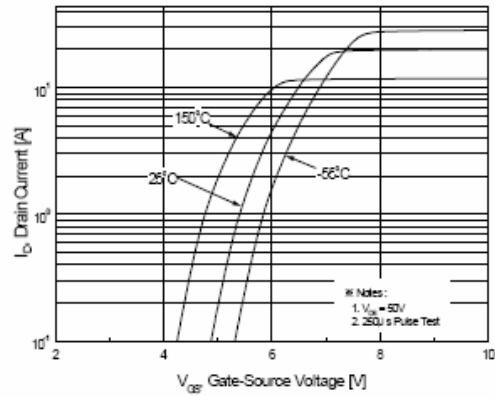


Fig.2 Transfer Current Characteristics

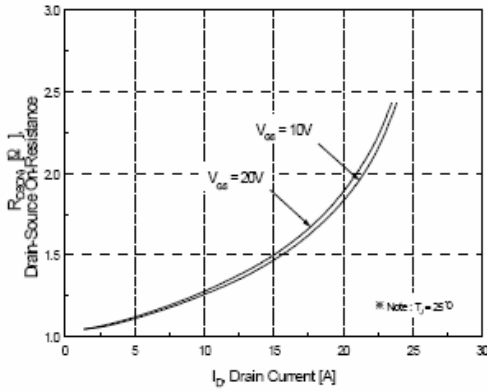


Fig.3 On-Resistance Variation vs Drain Current

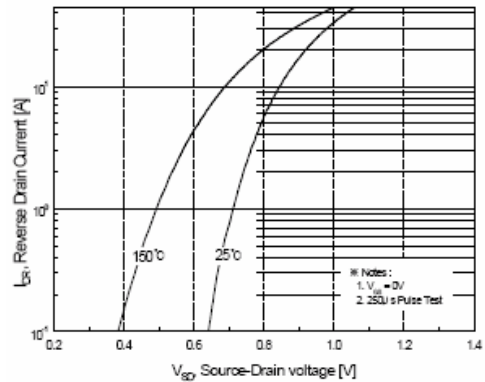


Fig.4 Body Diode Forward Voltage Variation with Source Current and Temperature

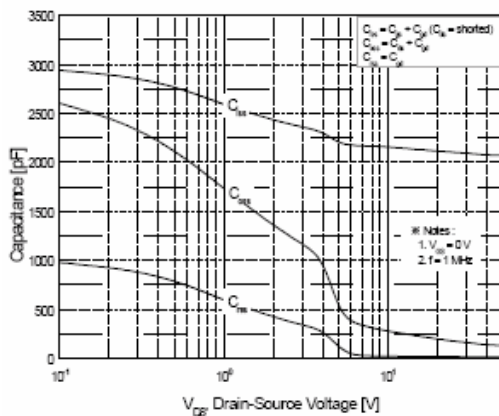


Fig.5 Capacitance Characteristics

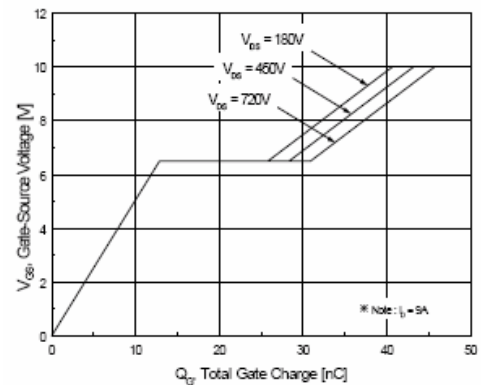


Fig.6 Gate Charge Characteristics

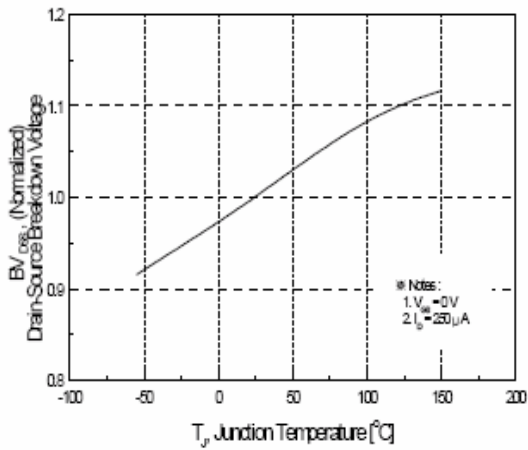


Fig.7 Breakdown Voltage Variation

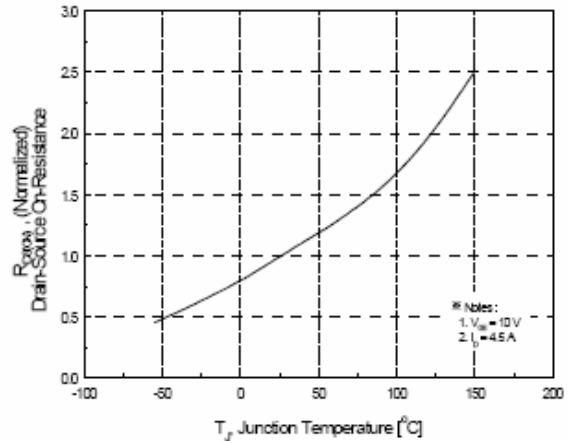


Fig.8 On-Resistance Variation vs. Temperature

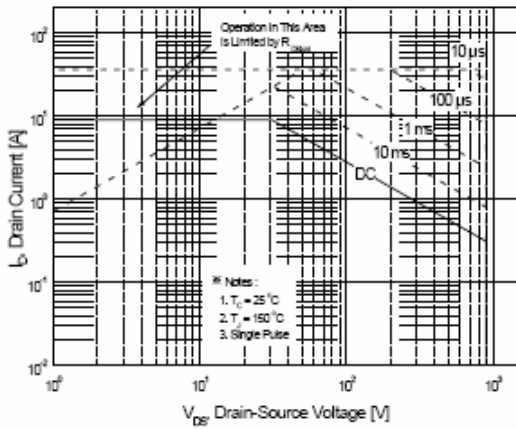


Fig.9 Maximum Safe Operation Area

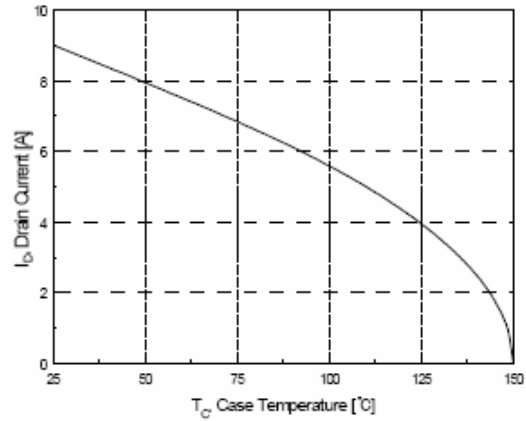


Fig.10 Maximum Drain Current vs Case Temperature

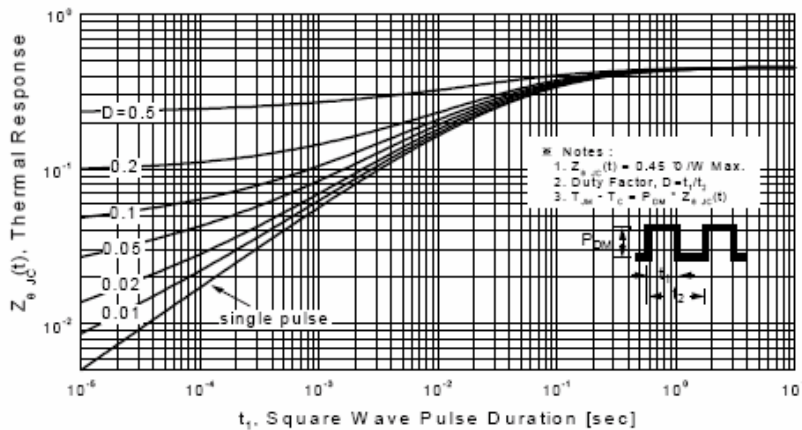


Fig.11 Transient Thermal Response Curve

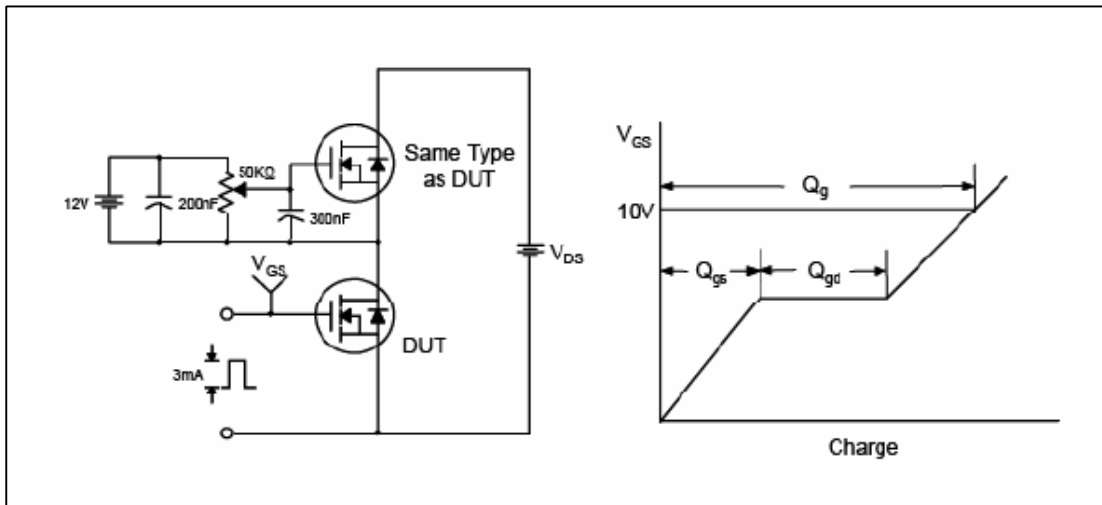


Fig.12 Gate Test Circuit & Waveform

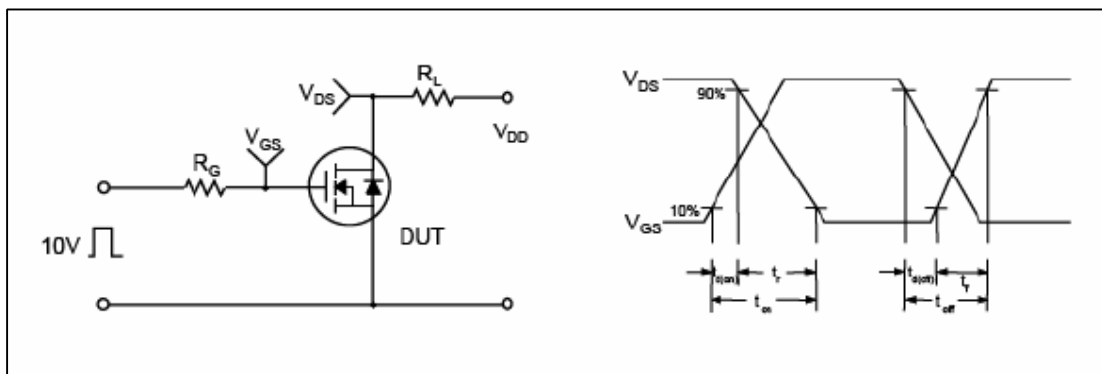


Fig.13 Resistive Switching Test Circuit & Waveform

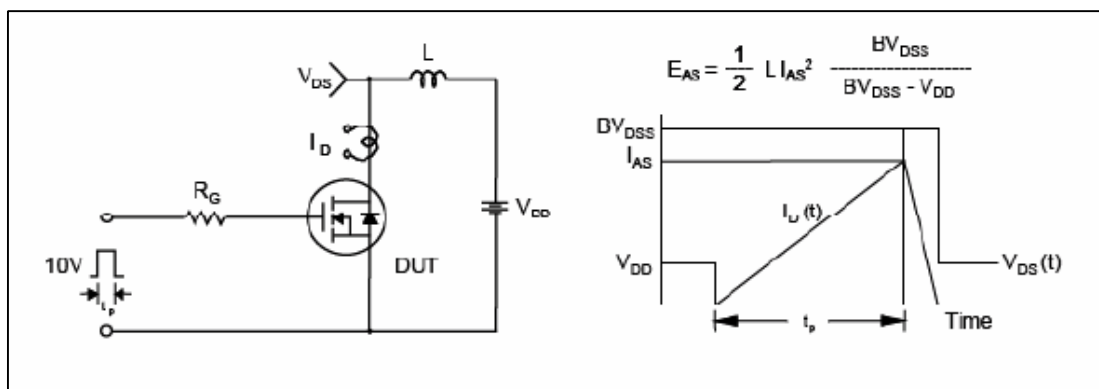


Fig.14 Unclamped Inductive Switching Test Circuit & Waveform

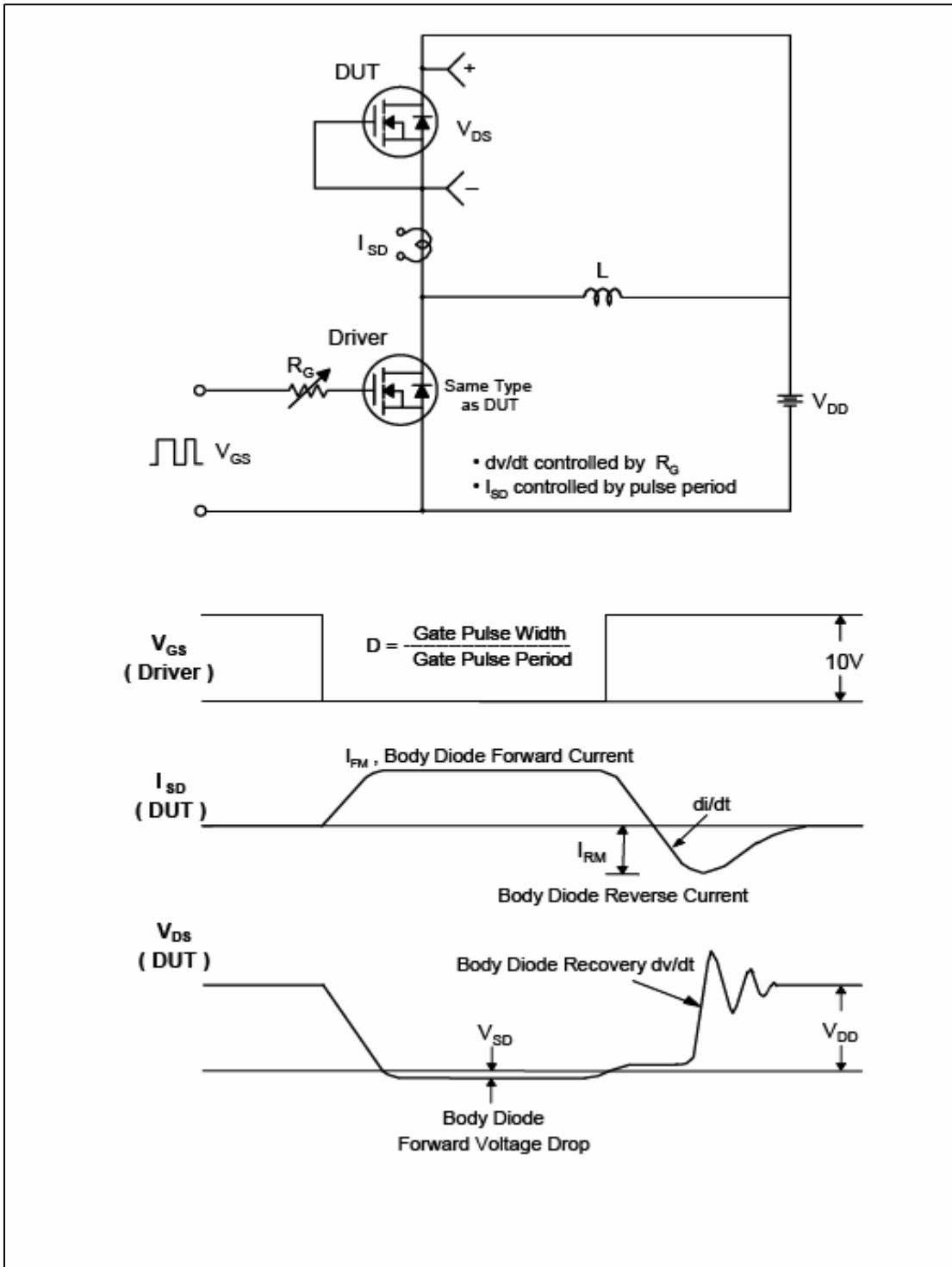


Fig.15 Peak Diode Recovery dv/dt Test Circuit & Waveform

TO-3PN Package Dimension

