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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# **DATA SHEET**

# MOS FIELD EFFECT TRANSISTOR Phase-out/Discontinued 2SK3455

# **SWITCHING** N-CHANNEL POWER MOS FET

### **DESCRIPTION**

The 2SK3455 is N-channel DMOS FET device that features a low gate charge and excellent switching characteristics, designed for high voltage applications such as switching power supply, AC adapter.

# **ORDERING INFORMATION**

PART NUMBER	PACKAGE
2SK3455	Isolated TO-220

# **FEATURES**

•Low gate charge

 $Q_G = 30 \text{ nC TYP.}$  ( $V_{DD} = 400 \text{ V}$ ,  $V_{GS} = 10 \text{ V}$ ,  $I_D = 12 \text{ A}$ )

- •Gate voltage rating ±30 V
- •Low on-state resistance

 $R_{DS(on)} = 0.60 \Omega MAX$ . (Vgs = 10 V, ID = 6.0 A)

- Avalanche capability ratings
- •Isolated TO-220 package

### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	500	٧
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	$V_{\text{GSS}}$	±30	V
Drain Current (DC) (Tc = 25°C)	$I_{D(DC)}$	±12	Α
Drain Current (Pulse) Note1	I <sub>D(pulse)</sub>	±36	Α
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T1</sub>	2.0	W
Total Power Dissipation (Tc = 25°C)	P <sub>T2</sub>	50	W
Channel Temperature	$T_ch$	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current Note2	I <sub>AS</sub>	12	Α
Single Avalanche Energy Note2	Eas	103	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

2. Starting  $T_{ch} = 25^{\circ}C$ ,  $V_{DD} = 150 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \rightarrow 0 \text{ V}$ 

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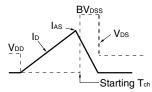


**ELECTRICAL CHARACTERISTICS (TA = 25°C)** 

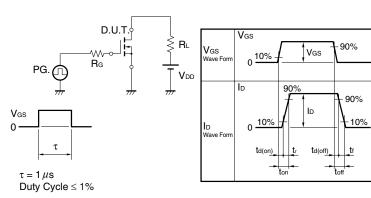
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V			100	μА
Gate Leakage Current	Igss	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V			±100	nA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	2.5		3.5	V
Forward Transfer Admittance	<b>y</b> fs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6.0 A	2.0			S
Drain to Source On-state Resistance	RDS(on)	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.0 A		0.50	0.60	Ω
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		1620		pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		250		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		10		pF
Turn-on Delay Time	td(on)	V <sub>DD</sub> = 150 V, I <sub>D</sub> = 6.0 A		24		ns
Rise Time	tr	V <sub>GS</sub> = 10 V		18		ns
Turn-off Delay Time	td(off)	R <sub>G</sub> = 10 Ω		50		ns
Fall Time	tr			15		ns
Total Gate Charge	QG	V <sub>DD</sub> = 400 V		30		nC
Gate to Source Charge	Qgs	V <sub>GS</sub> = 10 V		9		nC
Gate to Drain Charge	Q <sub>GD</sub>	ID = 12 A		11		nC
Body Diode Forward Voltage	VF(S-D)	IF = 12 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 12 A, VGS = 0 V		1.5		μS
Reverse Recovery Charge	Qrr	di/dt = 50 A/ μs		11		μC

# **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $\begin{array}{c} D.U.T. \\ R_G = 25 \Omega \\ V_{GS} = 20 \rightarrow 0 V \end{array}$ $\begin{array}{c} V_{DD} \\ V_{DD} \\ V_{DD} \end{array}$



# TEST CIRCUIT 2 SWITCHING TIME



# **TEST CIRCUIT 3 GATE CHARGE**

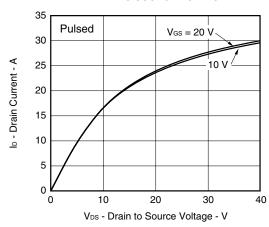
$$\begin{array}{c|c} D.U.T. \\ I_G = 2 \begin{array}{c} mA \\ \hline \end{array} \\ PG. \\ \begin{array}{c} \\ \\ \\ \end{array} \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \end{array} \begin{array}{c} \\ \\ \\ \end{array} \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \end{array} \begin{array}{c} \\ \\ \\ \end{array} \\ \end{array} \begin{array}{c} \\ \\ \\ \\ \end{array} \begin{array}{c} \\ \\ \\ \end{array} \\ V_{DD} \\ \end{array}$$



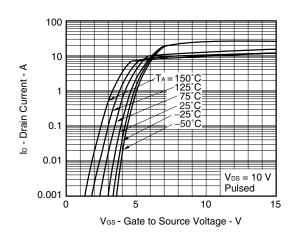
**Phase-out/Discontinued** 

# TYPICAL CHARACTERISTICS (TA = 25°C)

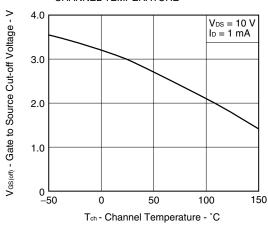
### DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



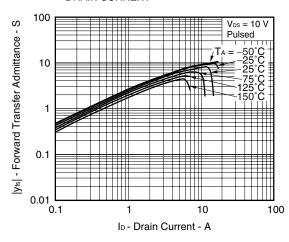
### FORWARD TRANSFER CHARACTERISTICS



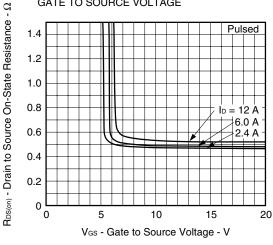
# GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



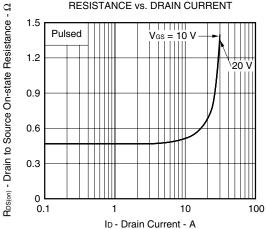
# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

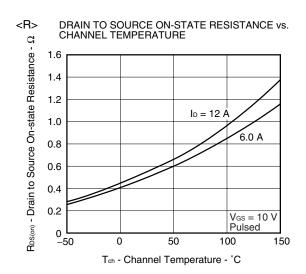


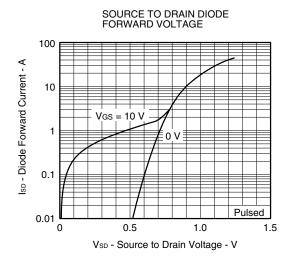
### DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

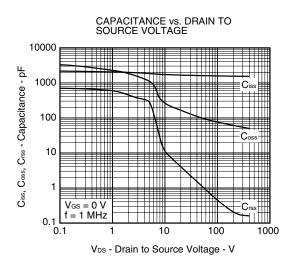


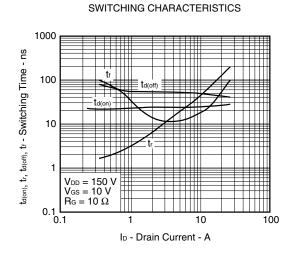


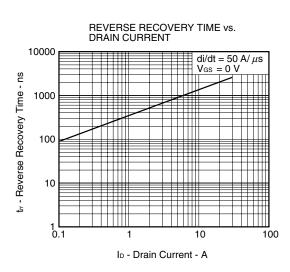
# Phase-out/Discontinued

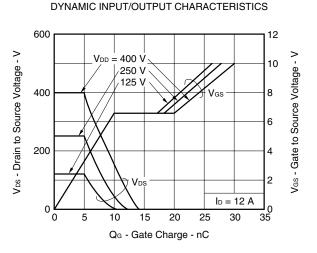






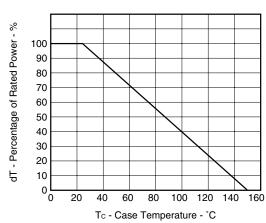








### DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

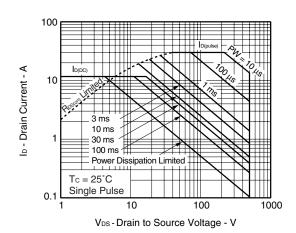


# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE 70 P<sub>T</sub> - Total Power Dissipation - W 60 50 40 30

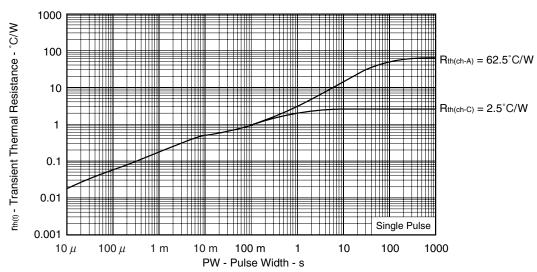
20 10 0 L 20 40 100 140 160

Tc - Case Temperature - °C

### FORWARD BIAS SAFE OPERATING AREA

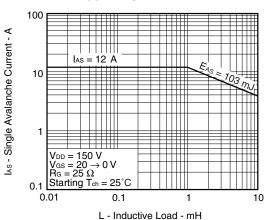


### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

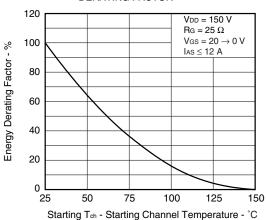




# SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



# SINGLE AVALANCHE ENERGY DERATING FACTOR

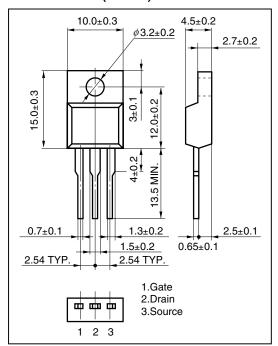


6

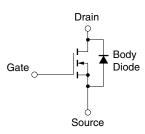


# **PACKAGE DRAWING (Unit: mm)**

# Isolated TO-220 (MP-45F)



# **EQUIVALENT CIRCUIT**



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.



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