

To our customers,

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## Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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EOL announced product

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## 2SK2978

Silicon N Channel MOS FET  
High Speed Power Switching

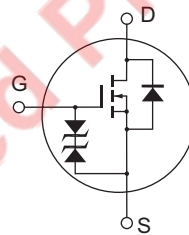
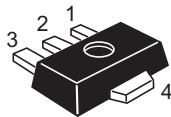
REJ03G1060-0500  
(Previous: ADE-208-659C)  
Rev.5.00  
Sep.07,2005

### Features

- Low on-resistance  
 $R_{DS(on)} = 0.09 \Omega$  typ. ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 1.5 \text{ A}$ )
- Low drive current
- High speed switching
- 2.5 V gate drive devices.

### Outline

RENESAS Package code: PLZZ0004CA-A  
(Package name: UPAK<sup>®</sup>)



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "ZY"

\*UPAK is a trademark of Renesas Technology Corp.

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V <sub>DSS</sub>	20	V
Gate to source voltage	V <sub>GSS</sub>	±10	V
Drain current	I <sub>D</sub>	2.5	A
Drain peak current	I <sub>D(pulse)</sub> <sup>Note1</sup>	5	A
Body-drain diode reverse drain current	I <sub>DR</sub>	2.5	A
Channel dissipation	P <sub>ch</sub> <sup>Note2</sup>	1	W
Channel temperature	T <sub>ch</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Notes: 1. PW ≤ 10μs, duty cycle ≤ 1 %

2. When using the alumina ceramic board (12.5 x 20 x 0.7 mm)

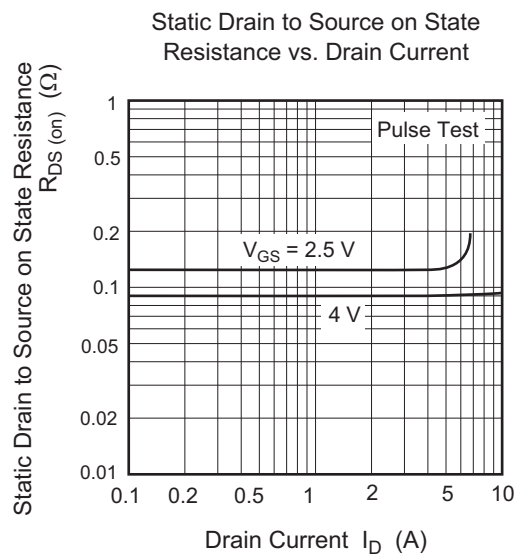
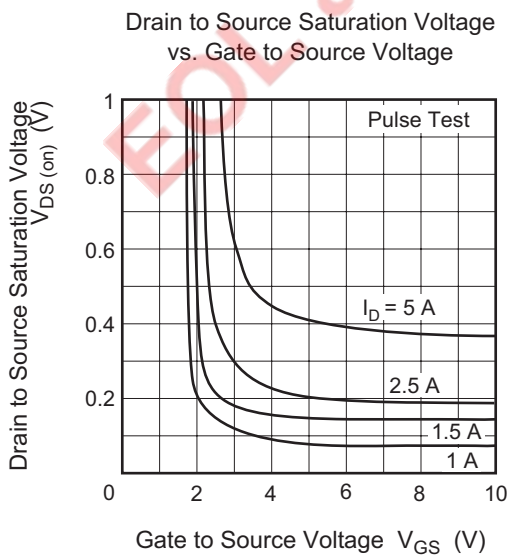
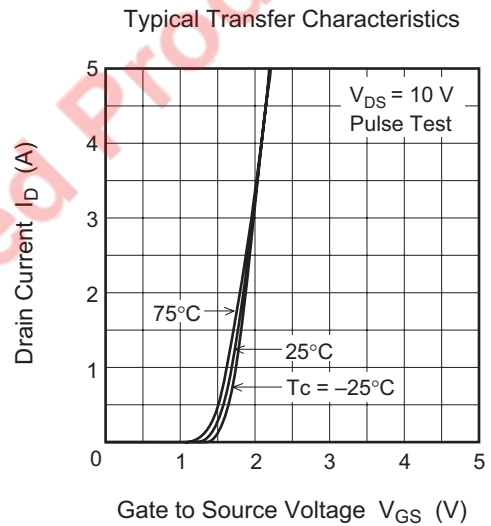
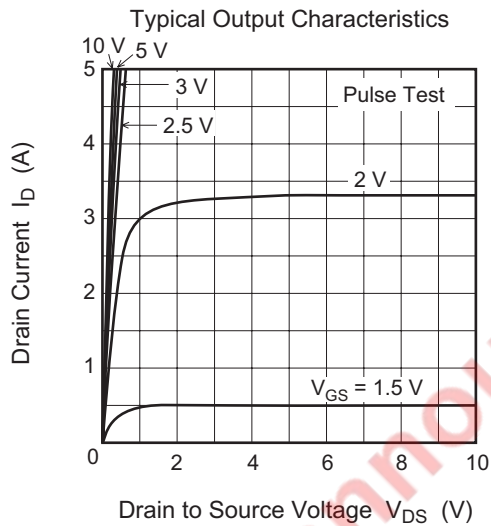
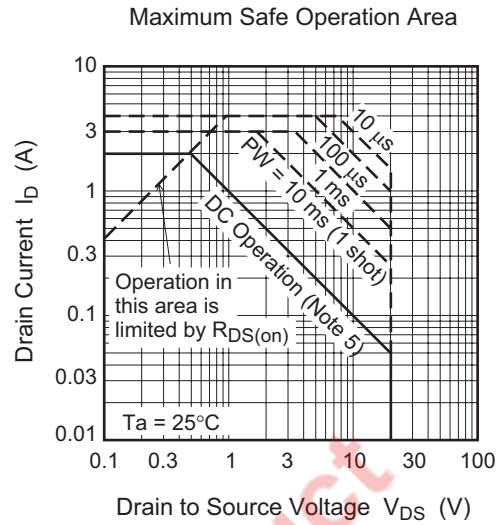
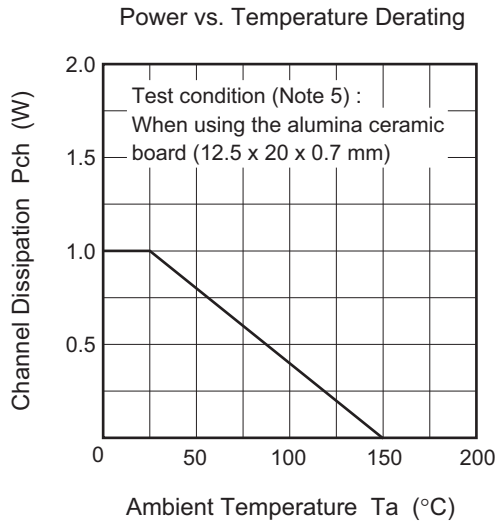
## Electrical Characteristics

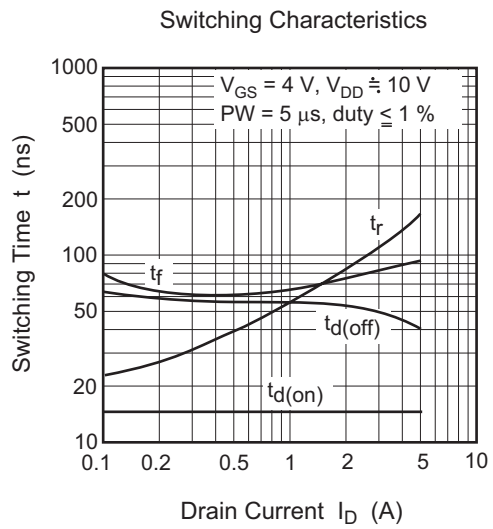
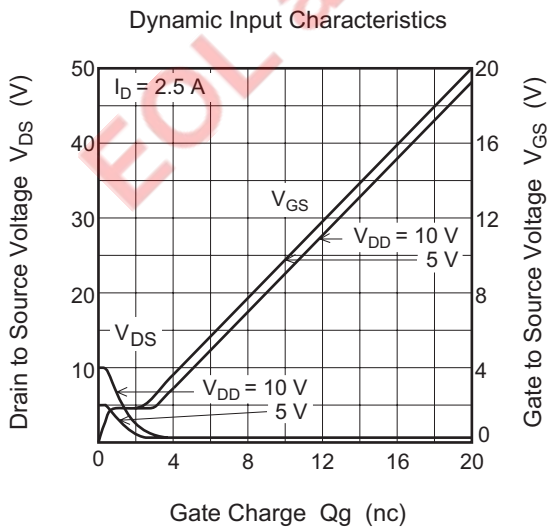
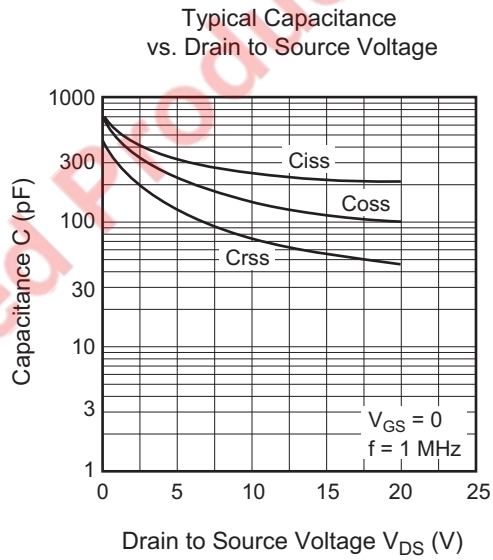
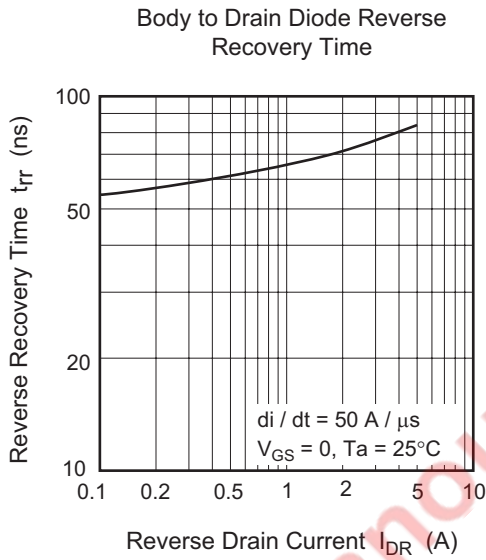
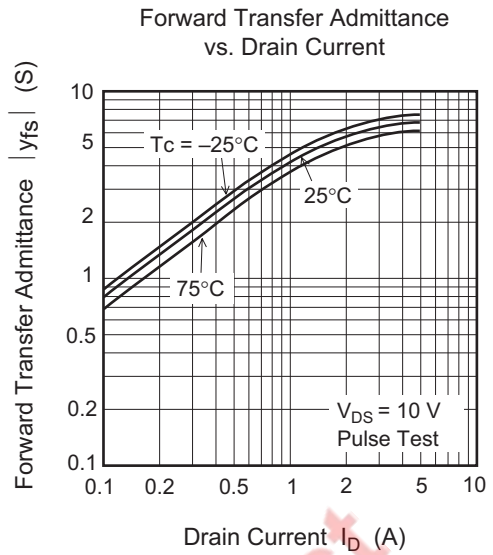
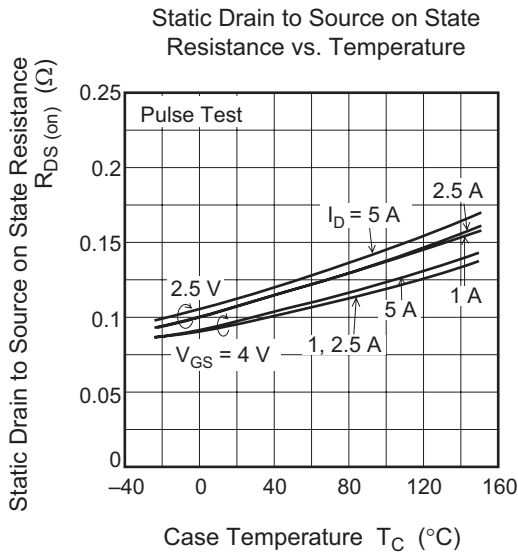
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V <sub>(BR)DSS</sub>	20	—	—	V	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0
Gate to source breakdown voltage	V <sub>(BR)GSS</sub>	±10	—	—	V	I <sub>G</sub> = ±100 μA, V <sub>DS</sub> = 0
Zero gate voltage drain current	I <sub>DSS</sub>	—	—	10	μA	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0
Gate to source leak current	I <sub>GSS</sub>	—	—	±10	μA	V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0
Gate to source cutoff voltage	V <sub>GS(off)</sub>	0.5	—	1.5	V	I <sub>D</sub> = 1 mA, V <sub>DS</sub> = 10 V
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	0.09	0.12	Ω	I <sub>D</sub> = 1.5 A, V <sub>GS</sub> = 4 V <sup>Note3</sup>
Static drain to source on state resistance	R <sub>DS(on)</sub>	—	0.12	0.20	Ω	I <sub>D</sub> = 1.5 A, V <sub>GS</sub> = 2.5 V <sup>Note3</sup>
Forward transfer admittance	y <sub>fs</sub>	3.0	5.0	—	S	I <sub>D</sub> = 1.5 A, V <sub>DS</sub> = 10 V <sup>Note3</sup>
Input capacitance	C <sub>iss</sub>	—	260	—	pF	V <sub>DS</sub> = 10 V, V <sub>GS</sub> = 0, f = 1 MHz
Output capacitance	C <sub>oss</sub>	—	150	—	pF	
Reverse transfer capacitance	C <sub>rss</sub>	—	75	—	pF	
Turn-on delay time	t <sub>d(on)</sub>	—	15	—	ns	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 1.5 A, R <sub>L</sub> = 6.67 Ω
Rise time	t <sub>r</sub>	—	70	—	ns	
Turn-off delay time	t <sub>d(off)</sub>	—	55	—	ns	
Fall time	t <sub>f</sub>	—	70	—	ns	
Body-drain diode forward voltage	V <sub>DF</sub>	—	0.9	—	V	I <sub>F</sub> = 2.5 A, V <sub>GS</sub> = 0
Body-drain diode reverse recovery time	t <sub>rr</sub>	—	75	—	ns	I <sub>F</sub> = 2.5 A, V <sub>GS</sub> = 0 di <sub>F</sub> /dt = 50 A/μs

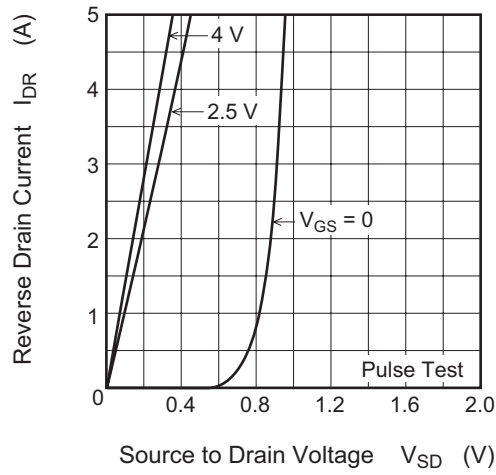
Note: 3. Pulse test

Main Characteristics

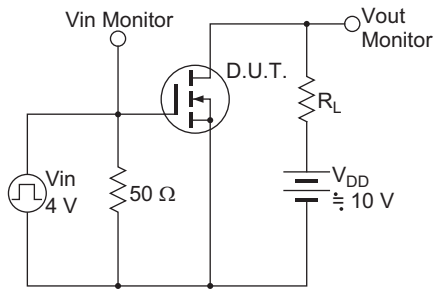




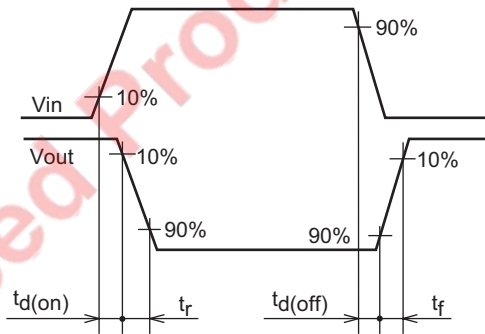
Reverse Drain Current vs. Source to Drain Voltage



Switching Time Test Circuit

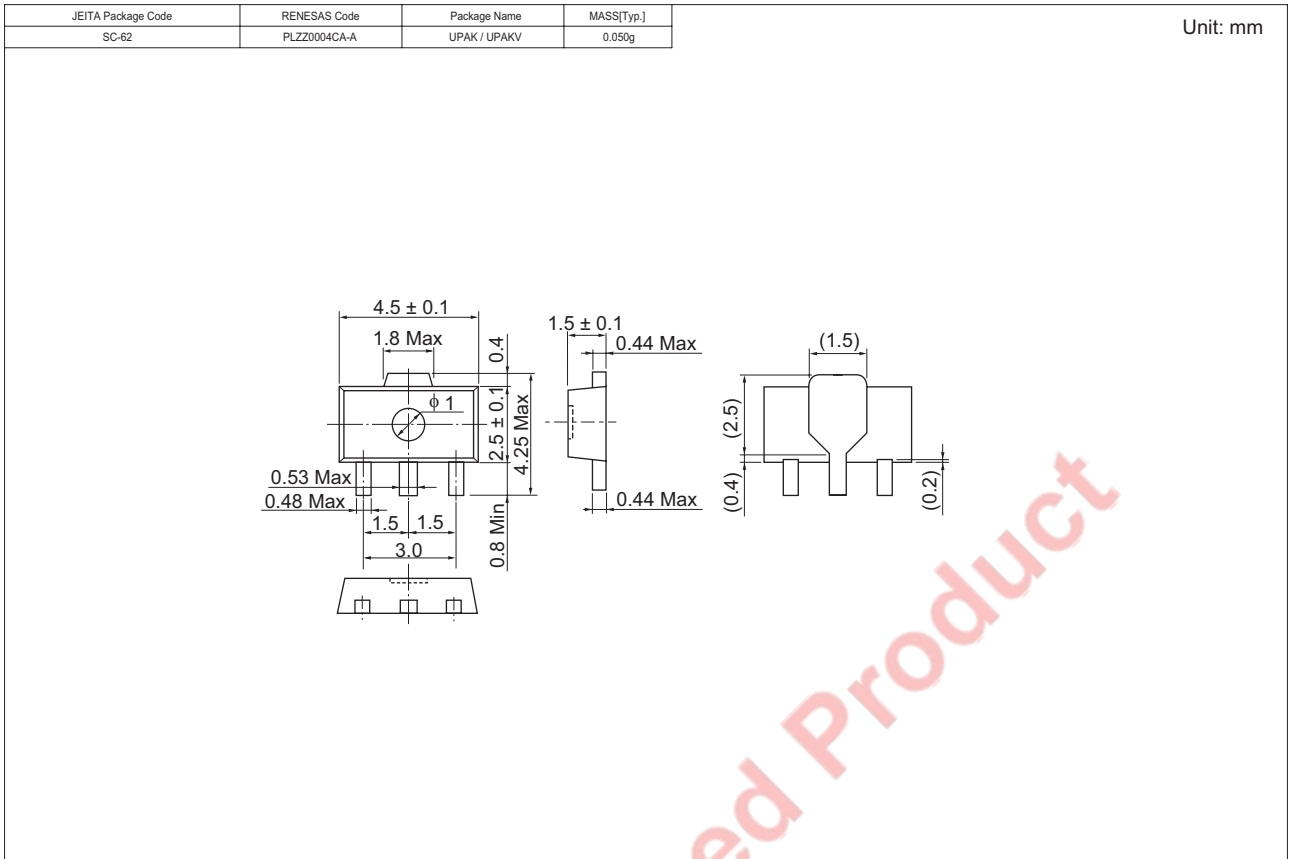


Waveform



EOL announced Product

### Package Dimensions



### Ordering Information

Part Name	Quantity	Shipping Container
2SK2978ZYTL-E	1000 pcs	Taping
2SK2978ZYTR-E	1000 pcs	Taping

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