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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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2SK2730

Silicon N Channel MOS FET
High Speed Power Switching

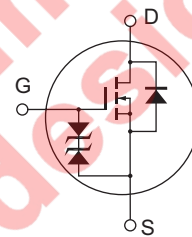
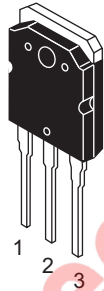
REJ03G1028-0300
(Previous: ADE-208-493A)
Rev.3.00
Sep 07, 2005

Features

- Low on-resistance
- High speed switching
- Low drive current
- Avalanche ratings

Outline

RENESAS Package code: PRSS0004ZE-A
(Package name: TO-3P)



1. Gate
2. Drain (Flange)
3. Source

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	500	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}^{*1}$	100	A
Body to drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP}^{*3}	25	A
Avalanche energy	E_{AR}^{*3}	35	mJ
Channel dissipation	P_{ch}^{*2}	175	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

- Notes: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

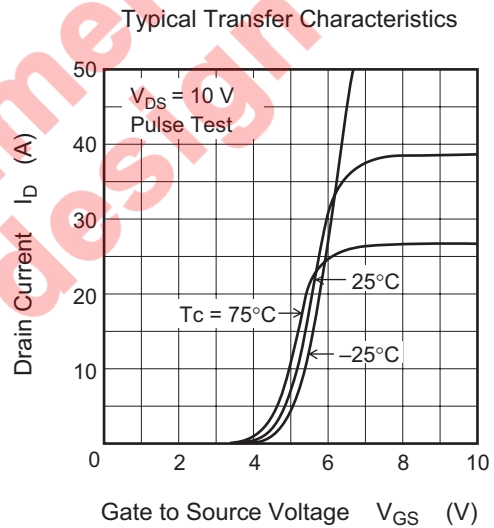
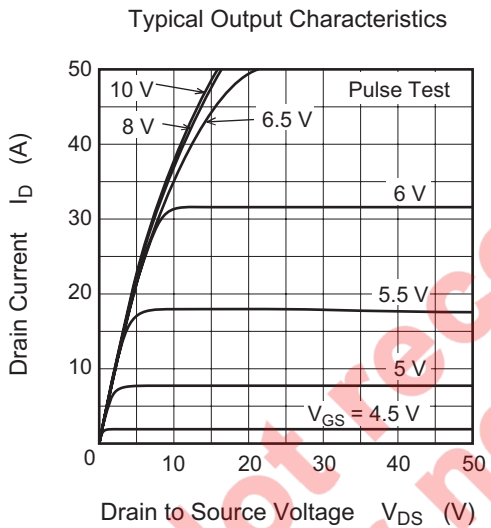
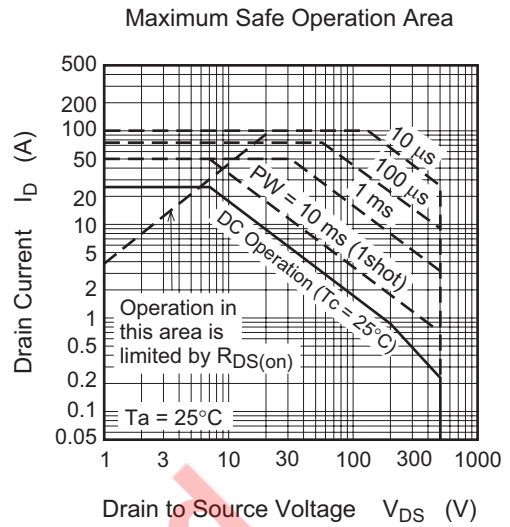
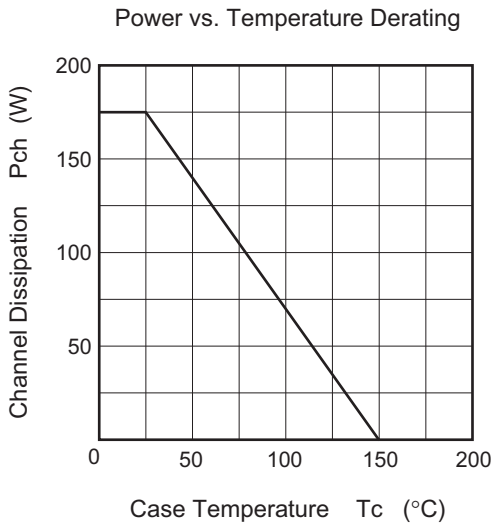
Electrical Characteristics

(Ta = 25°C)

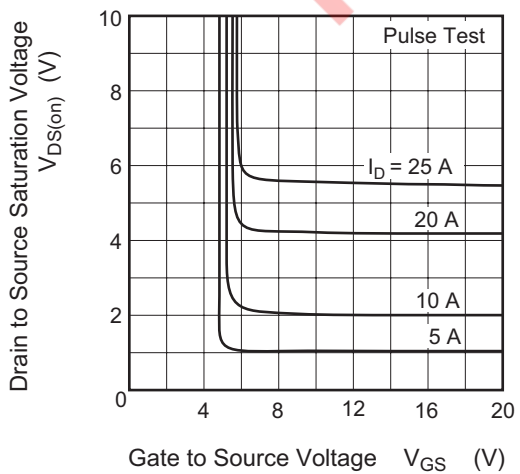
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±30	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 25 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 500 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.5	—	3.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}^{*4}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.2	0.24	Ω	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}^{*4}$
Forward transfer admittance	$ y_{fs} $	12	20	—	S	$I_D = 15 \text{ A}$, $V_{DS} = 10 \text{ V}^{*4}$
Input capacitance	C_{iss}	—	3500	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	1000	—	pF	
Reverse transfer capacitance	C_{rss}	—	150	—	pF	
Total gate charge	Q_g	—	65	—	nc	$V_{DD} = 400 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 25 \text{ A}$
Gate to source charge	Q_{gs}	—	16	—	nc	
Gate to drain charge	Q_{gd}	—	24	—	nc	
Turn-on delay time	$t_{d(on)}$	—	50	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$, $R_L = 2 \Omega$
Rise time	t_r	—	140	—	ns	
Turn-off delay time	$t_{d(off)}$	—	200	—	ns	
Fall time	t_f	—	110	—	ns	
Body to drain diode forward voltage	V_{DF}	—	1.1	—	V	$I_D = 25 \text{ A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	450	—	ns	$I_F = 25 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100A/\mu s$

- Note: 4. Pulse test

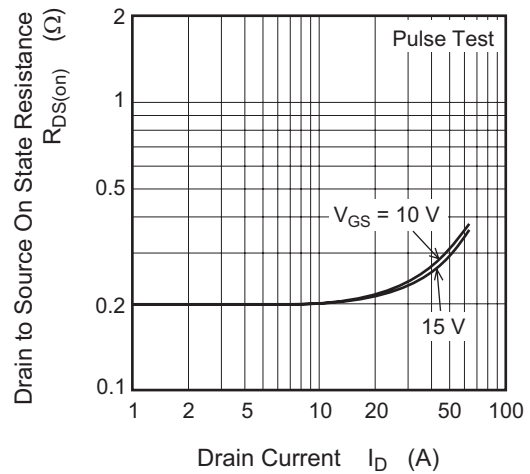
Main Characteristics

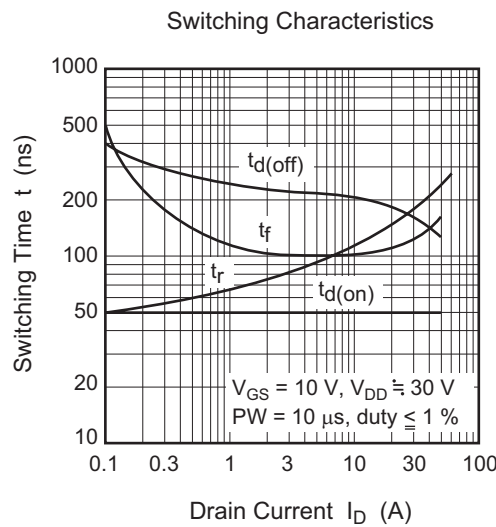
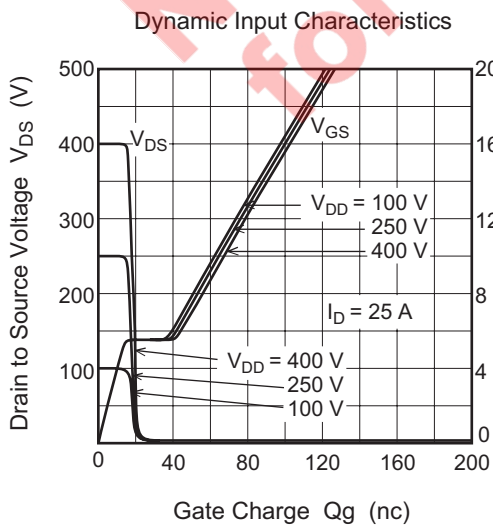
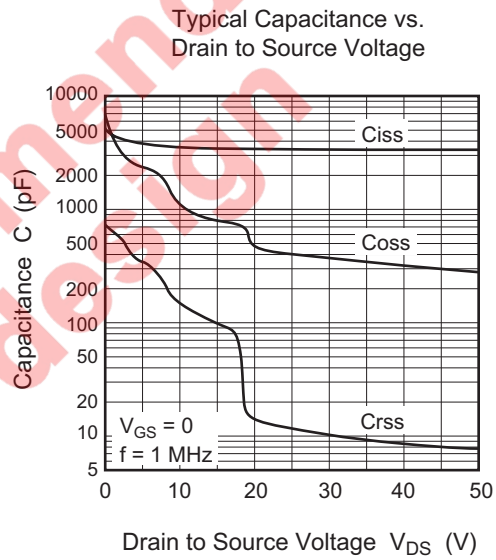
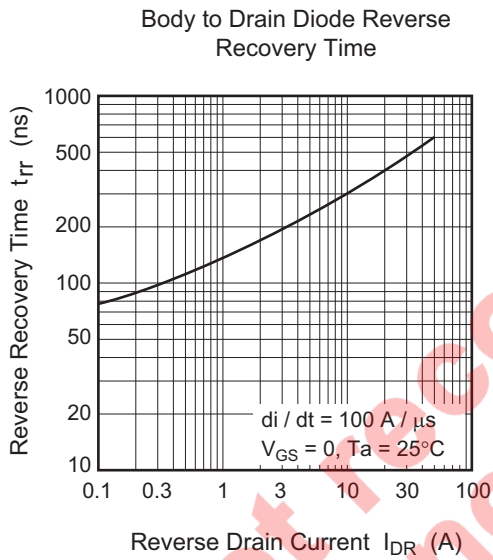
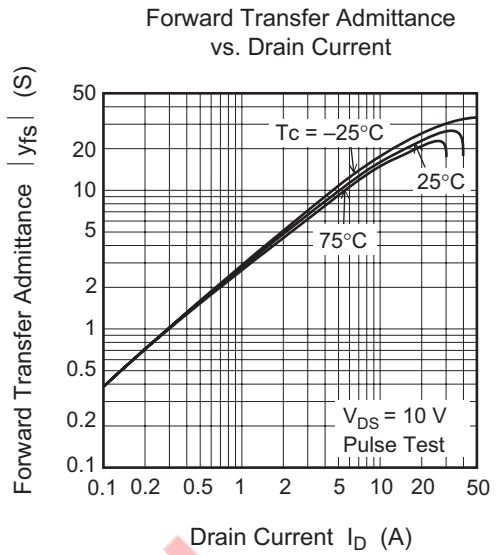
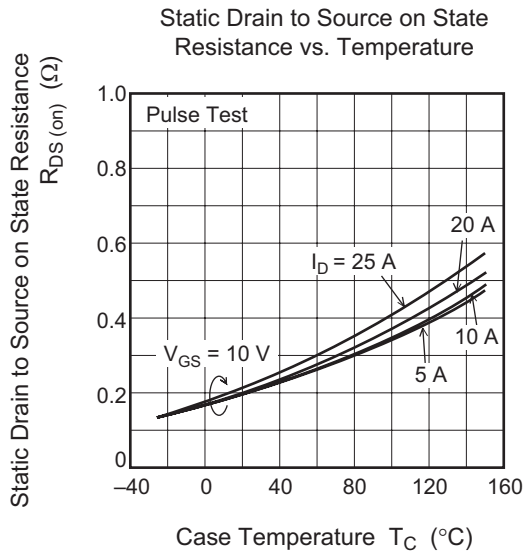


Drain to Source Saturation Voltage vs. Gate to Source Voltage

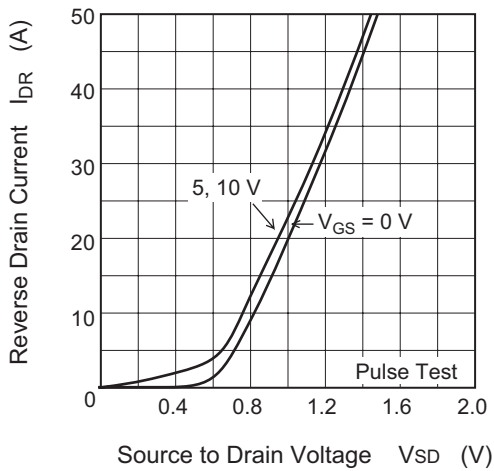


Static Drain to Source on State Resistance vs. Drain Current

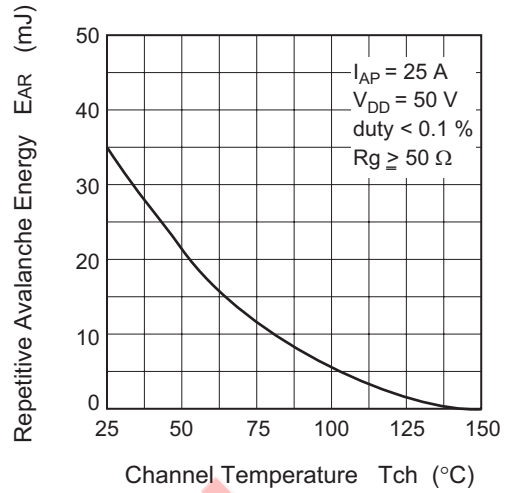




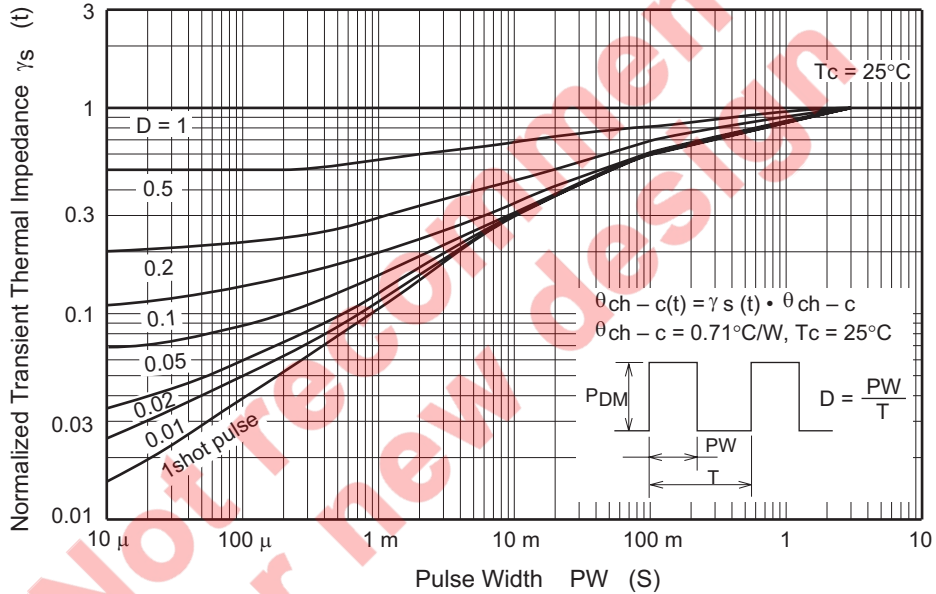
Reverse Drain Current vs. Source to Drain Voltage



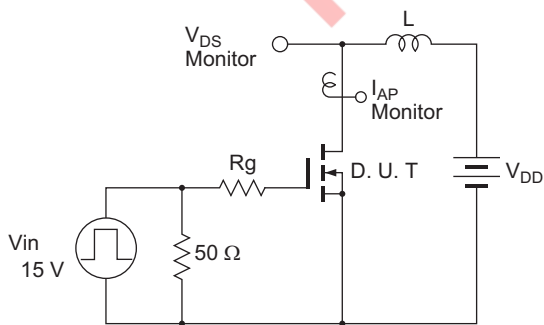
Maximum Avalanche Energy vs. Channel Temperature Derating



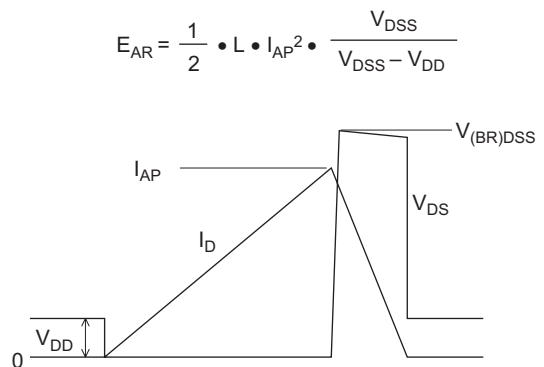
Normalized Transient Thermal Impedance vs. Pulse Width

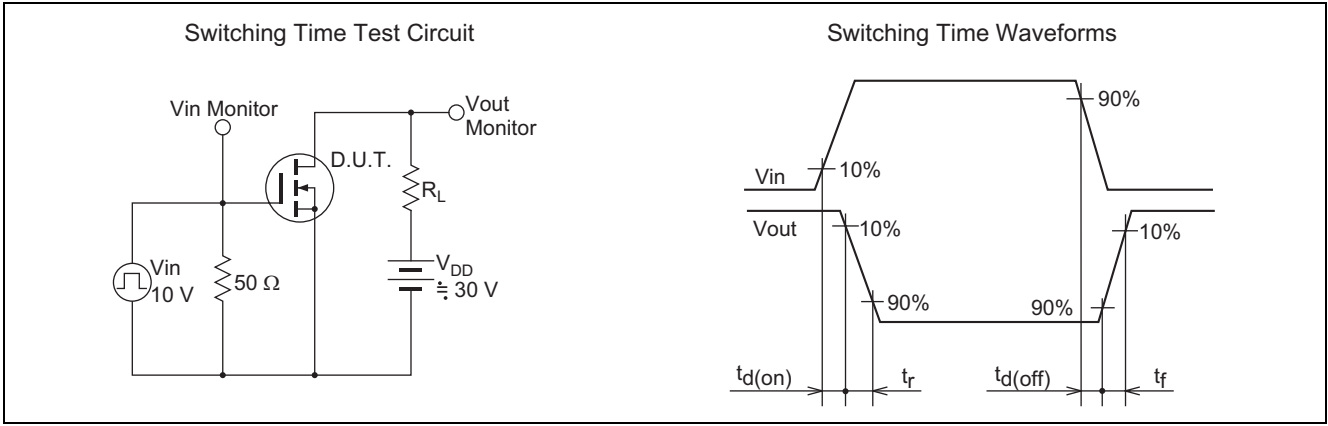


Avalanche Test Circuit



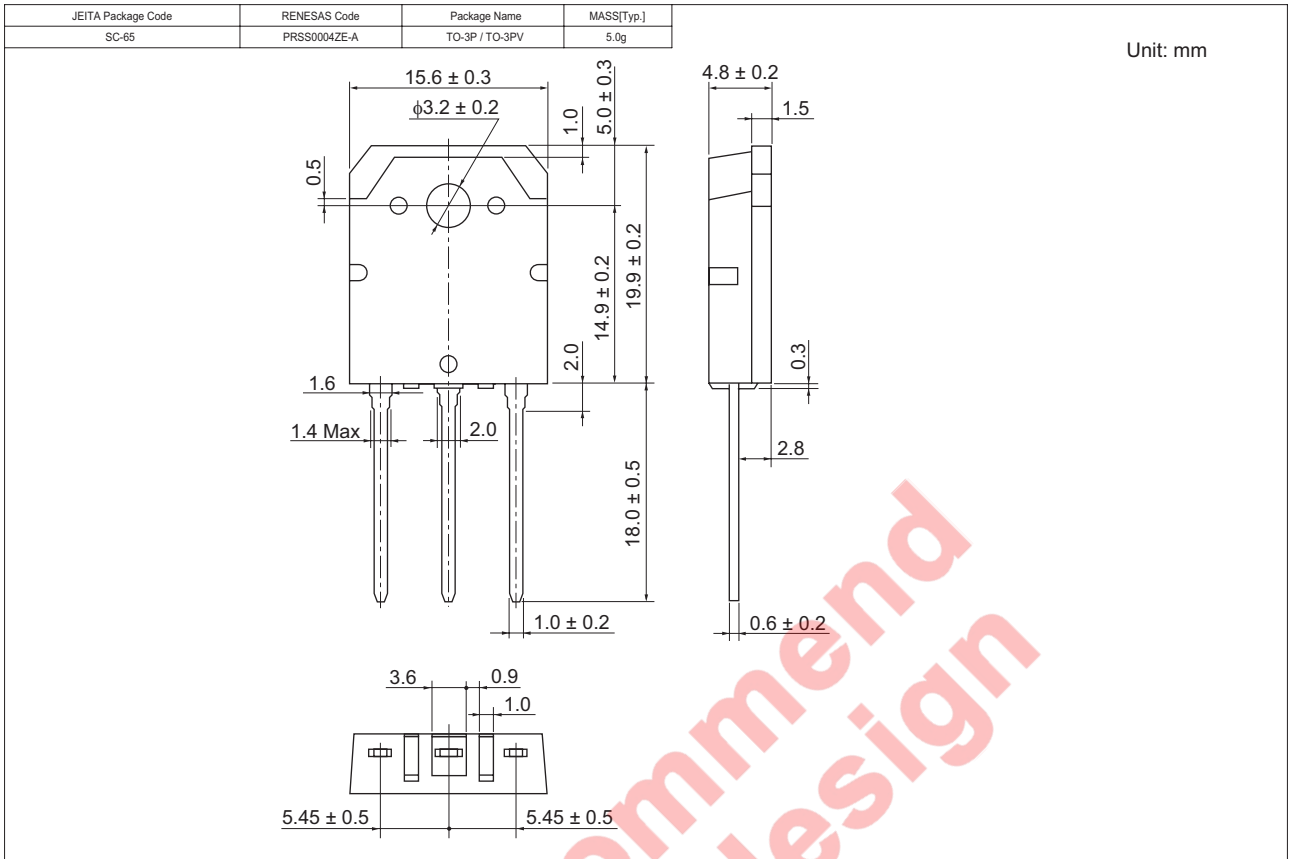
Avalanche Waveform





Not recommend
for new design

Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SK2730-E	360 pcs	Box (Tube)

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Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510