To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

Send any inquiries to http://www.renesas.com/inquiry.

RENESAS

RENESAS

MOS FIELD EFFECT TRANSISTOR
2SK2413

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2413 is N-Channel MOS Field Effect Transistor designed for high speed switching applications.

FEATURES

- Low On-Resistance
  $R_{DS(on)1}$ = 70 mΩ MAX. (@ V_{GS} = 10 V, I_D = 5.0 A)
  $R_{DS(on)2}$ = 95 mΩ MAX. (@ V_{GS} = 4 V, I_D = 5.0 A)
- Low C_{iss} C_{iss} = 860 pF TYP.
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

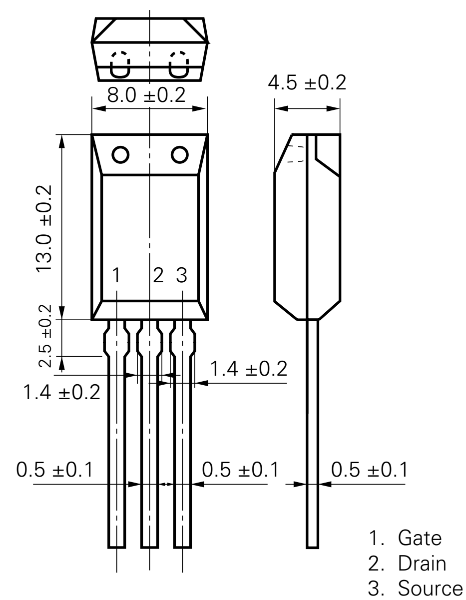
ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±10	A
Drain Current (pulse)*	$I_{D(pulse)}$	±40	A
Total Power Dissipation (T_A = 25 °C)	P_T	1.8	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current**	I_{AS}	10	A
Single Avalanche Energy**	E_{AS}	10	mJ

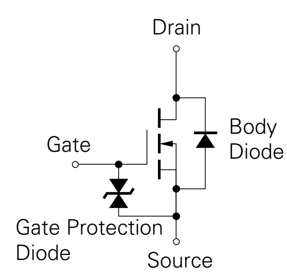
* PW ≤ 10 μs, Duty Cycle ≤ 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

PACKAGE DIMENSIONS
(in millimeter)



MP-10 (ISOLATED TO-220)



The information in this document is subject to change without notice.

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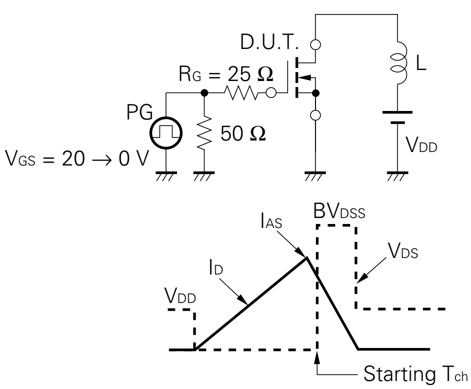
(O. D. No. TC-8032)
Date Published November 1994 P
Printed in Japan

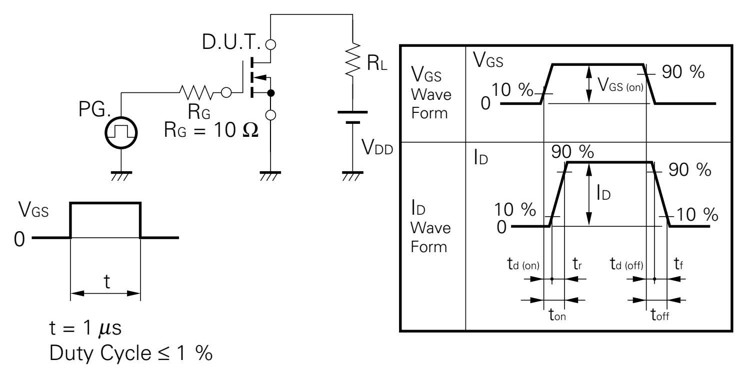
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	$R_{DS(on)1}$		50	70	mΩ	V_{GS} = 10 V, I_D = 5.0 A
Drain to Source On-Resistance	$R_{DS(on)2}$		70	95	mΩ	V_{GS} = 4 V, I_D = 5.0 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	1.0	1.6	2.0	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\lvert y_{fs} \rvert$	7.0	12		S	V_{DS} = 10 V, I_D = 5.0 A
Drain Leakage Current	I_{DSS}			±10	μA	V_{DS} = 60 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±20 V, V_{DS} = 0
Input Capacitance	C_{iss}		860		pF	V_{DS} = 10 V
Output Capacitance	C_{oss}		440		pF	V_{GS} = 0
Reverse Transfer Capacitance	C_{rss}		110		pF	f = 1 MHz
Turn-On Delay Time	$t_{d(on)}$		15		ns	I_D = 5.0 A
Rise Time	t_r		90		ns	$V_{GS(on)}$ = 10 V
Turn-Off Delay Time	$t_{d(off)}$		75		ns	V_{DD} = 30 V
Fall Time	t_f		30		ns	R_G = 10 Ω
Total Gate Charge	Q_G		24		nC	I_D = 20 A
Gate to Source Charge	Q_{GS}		3.0		nC	V_{DD} = 48 V
Gate to Drain Charge	Q_{GD}		6.0		nC	V_{GS} = 10 V
Body Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 10 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		95		ns	I_F = 10 A, V_{GS} = 0
Reverse Recovery Charge	Q_{rr}		250		nC	di/dt = 100 A/μs

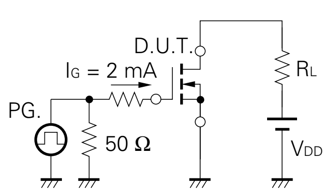
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time

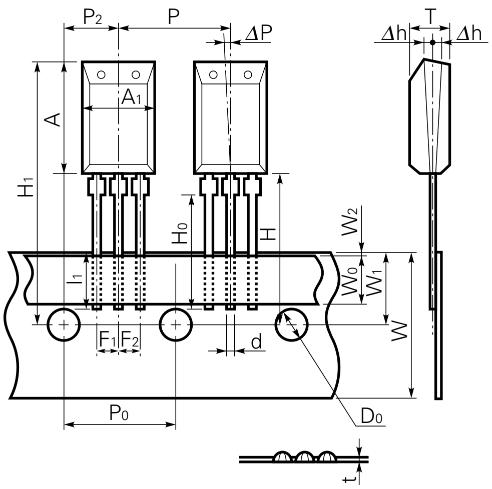


Test Circuit 3 Gate Charge



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

Radial Tape Specification

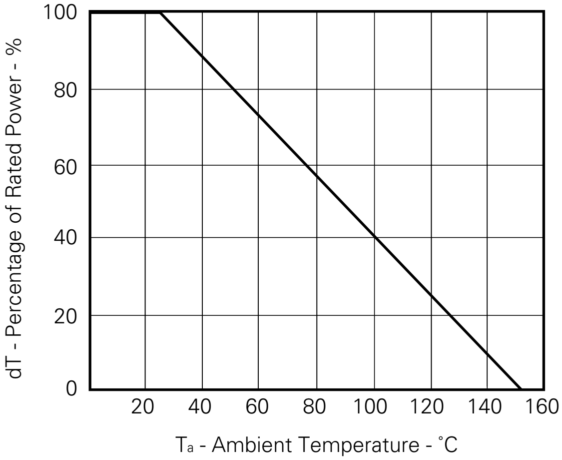


Dimension (unit: mm)

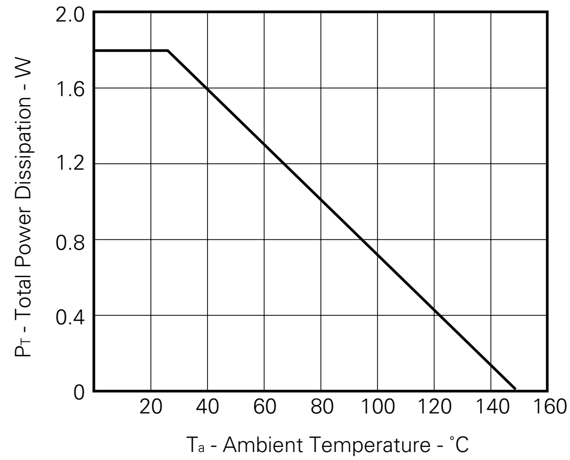
Item		
Component Body Length along Tape	A_1	8.0 ± 0.2
Component Body Height	A	13.0 ± 0.2
Component Body Width	T	4.5 ± 0.2
Component Lead Width Dimension	d	0.5 ± 0.1
Lead Wire Enclosure	I_1	2.5 MIN.
Component Center Pitch	P	12.7 ± 1.0
Feedhole Pitch	P_0	12.7 ± 0.3
Feedhole Center to Center Lead	P_2	6.35 ± 0.5
Component Lead Pitch	F_1, F_2	$2.5^{+0.4}_{-0.1}$
Deflection Front or Rear	Δh	±1.0
Deflection Left or Right	ΔP	±1.3
Carrier Strip Width	W	$18.0^{+1.0}_{-0.5}$
Adhesive Tape Width	W_0	5.0 MIN.
Feedhole Location	W_1	9.0 ± 0.5
Adhesive Tape Position	W_2	0.7 MIN.
Height of Seating Plane	H_0	16.0 ± 0.5
Feedhole to upper of Component	H_1	32.2 MAX.
Feedhole to Bottom of Component	H	20.0 MAX.
Tape Feedhole Diameter	D_0	4.0 ± 0.2
Overall Taped Package Thickness	t	0.7 ± 0.2

TYPICAL CHARACTERISTICS (T_A = 25 ˚C)

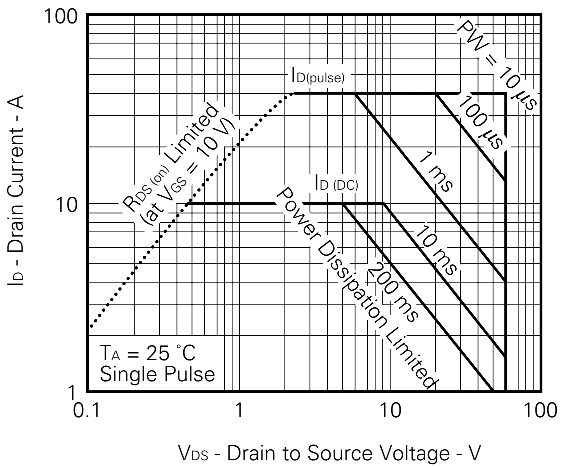
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



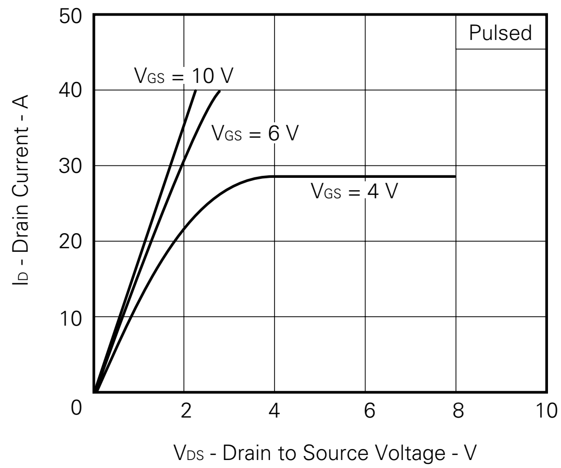
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



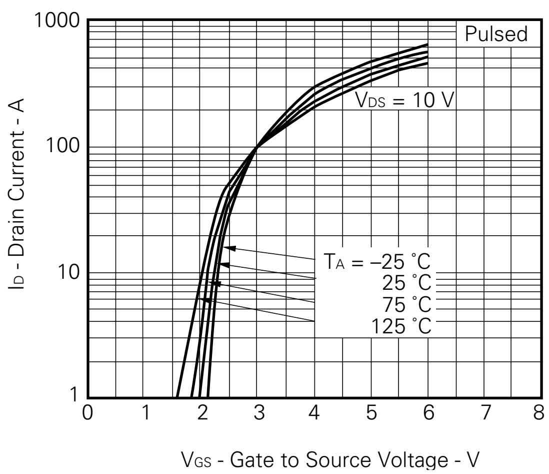
FORWARD BIAS SAFE OPERATING AREA



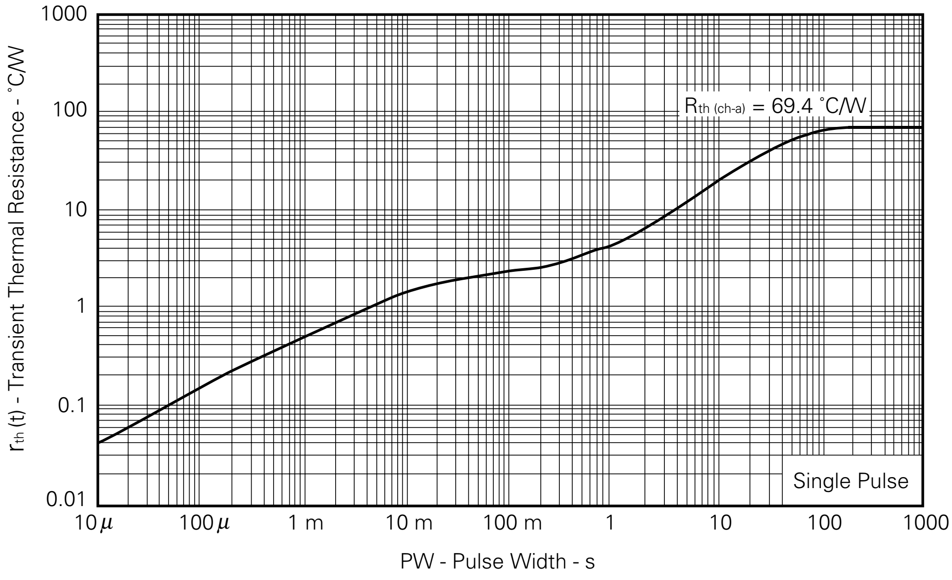
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



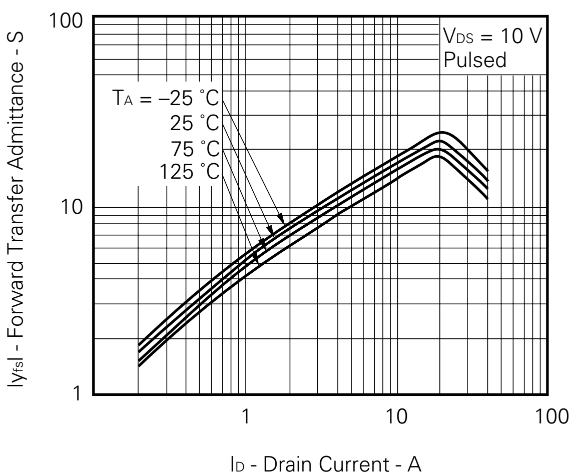
FORWARD TRANSFER CHARACTERISTICS



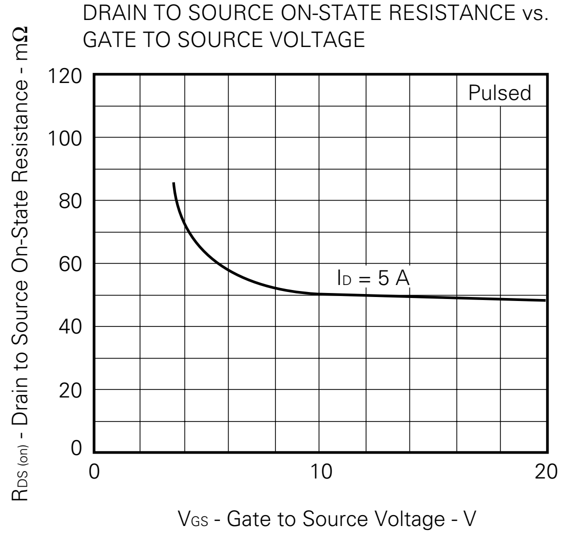
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



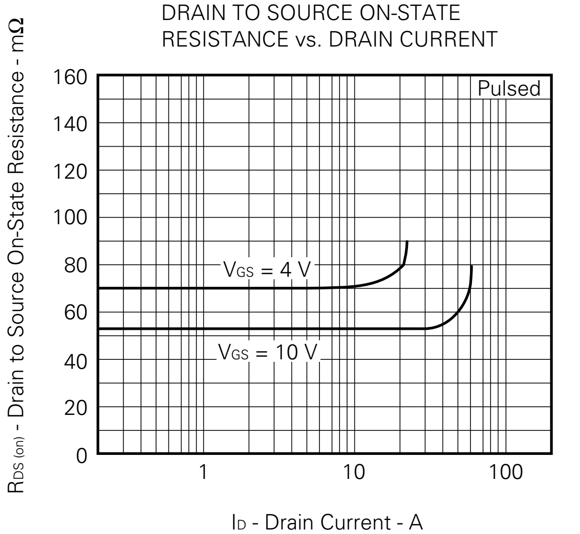
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



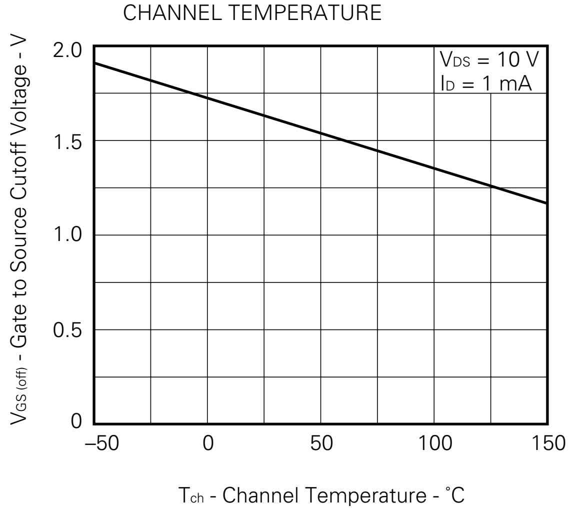
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



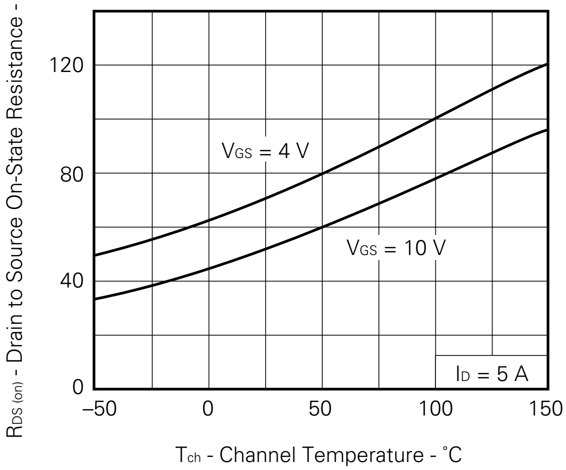
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



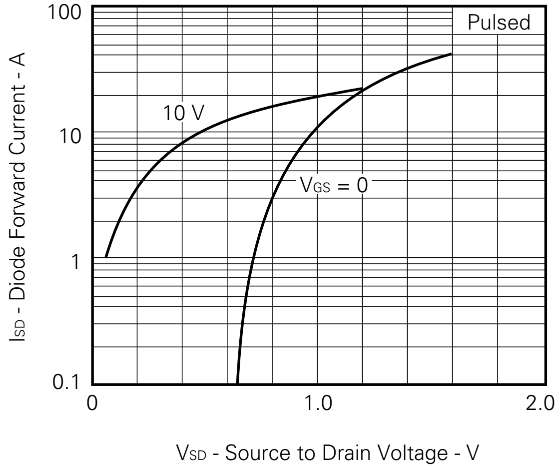
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



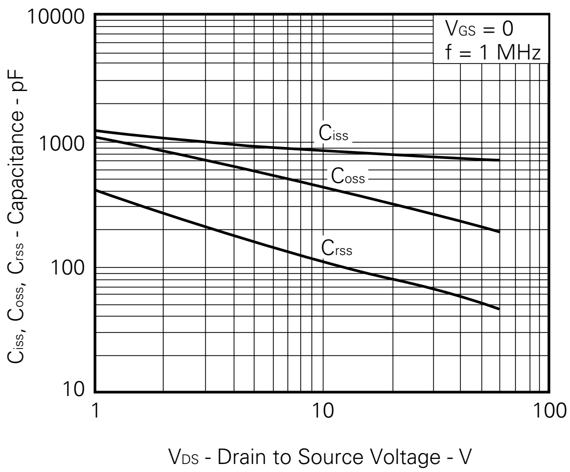
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



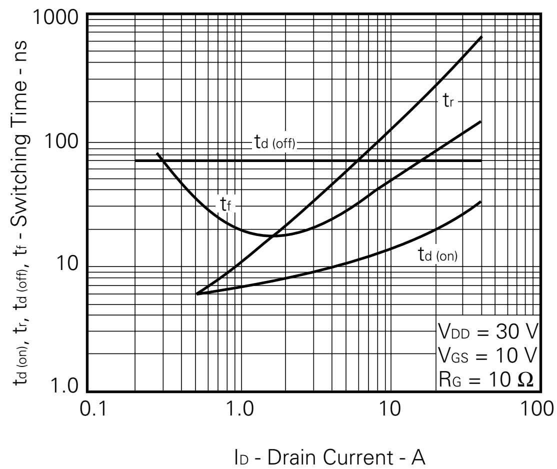
SOURCE TO DRAIN DIODE
FORWARD VOLTAGE



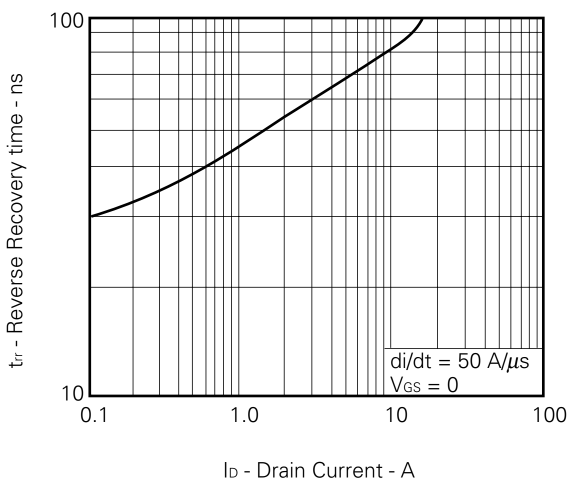
CAPACITANCE vs. DRAIN TO
SOURCE VOLTAGE



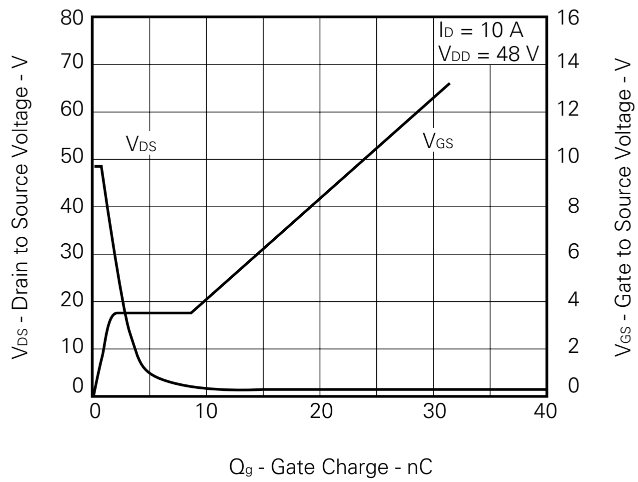
SWITCHING CHARACTERISTICS



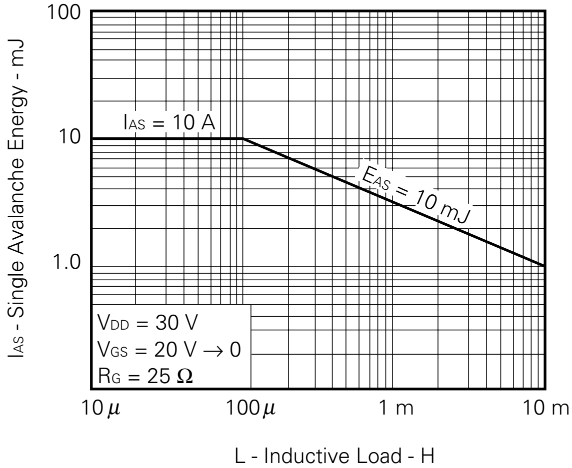
REVERSE RECOVERY TIME vs.
DRAIN CURRENT



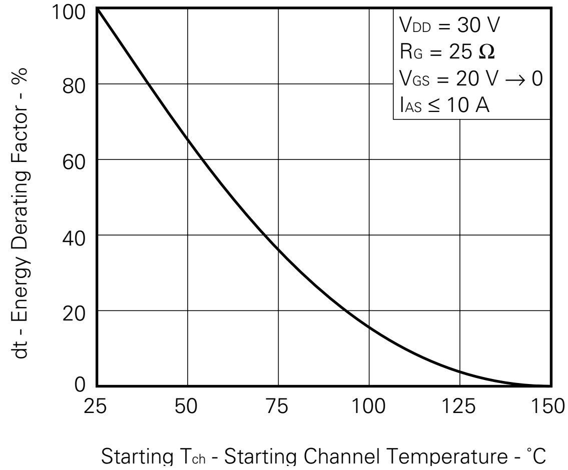
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE ENERGY vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

M4 92.6