

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR  
**2SK2413**

**SWITCHING  
 N-CHANNEL POWER MOS FET  
 INDUSTRIAL USE**

**DESCRIPTION**

The 2SK2413 is N-Channel MOS Field Effect Transistor designed for high speed switching applications.

**FEATURES**

- Low On-Resistance  
 $R_{DS(on)1} = 70 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 10 \text{ V, } I_D = 5.0 \text{ A)}$   
 $R_{DS(on)2} = 95 \text{ m}\Omega \text{ MAX. (@ } V_{GS} = 4 \text{ V, } I_D = 5.0 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 860 \text{ pF TYP.}$
- Built-in G-S Gate Protection Diodes
- High Avalanche Capability Ratings

**QUALITY GRADE**

Standard

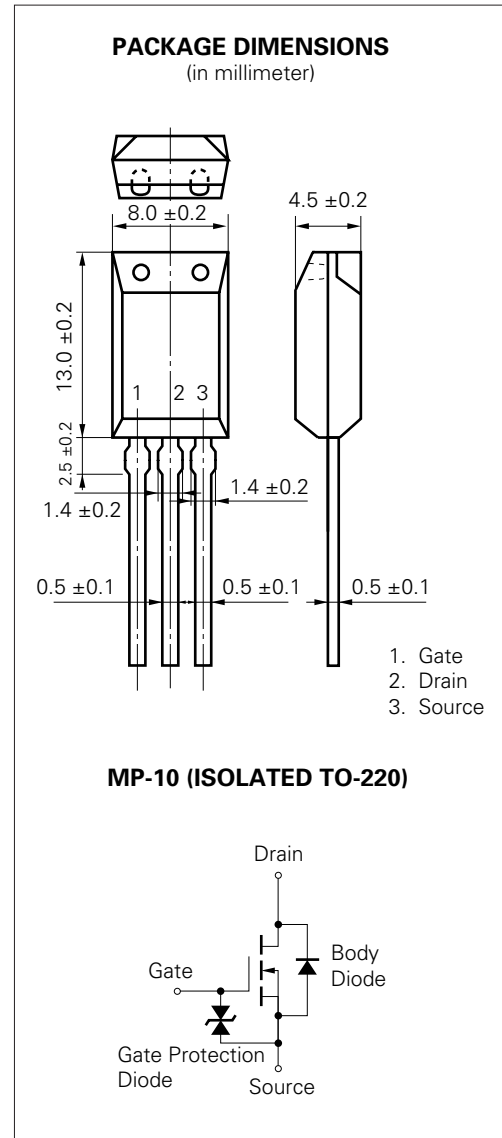
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

**ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)**

Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 10$	A
Drain Current (pulse)*	$I_{D(pulse)}$	$\pm 40$	A
Total Power Dissipation (TA = 25 °C)	$P_T$	1.8	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
Single Avalanche Current**	$I_{AS}$	10	A
Single Avalanche Energy**	$E_{AS}$	10	mJ

\*  $PW \leq 10 \mu s$ , Duty Cycle  $\leq 1 \%$

\*\* Starting  $T_{ch} = 25 \text{ °C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

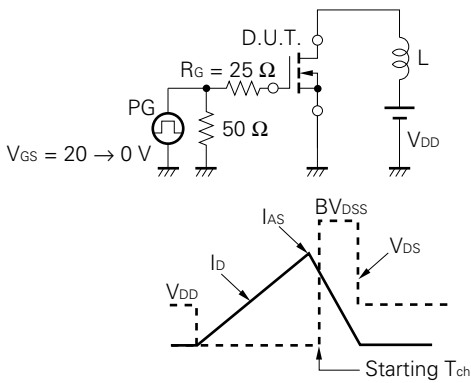


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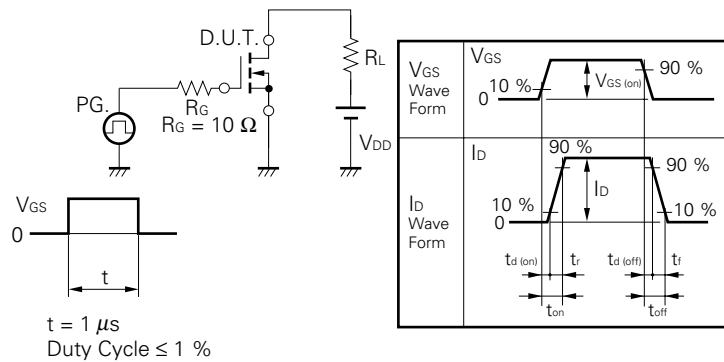
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	R <sub>DS(on)1</sub>		50	70	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 5.0 A
Drain to Source On-Resistance	R <sub>DS(on)2</sub>		70	95	mΩ	V <sub>GS</sub> = 4 V, I <sub>D</sub> = 5.0 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	1.0	1.6	2.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	7.0	12		S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A
Drain Leakage Current	I <sub>bss</sub>			±10	μA	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		860		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		440		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		110		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		15		ns	I <sub>D</sub> = 5.0 A
Rise Time	t <sub>r</sub>		90		ns	V <sub>GS(on)</sub> = 10 V
Turn-Off Delay Time	t <sub>d(off)</sub>		75		ns	V <sub>DD</sub> = 30 V
Fall Time	t <sub>f</sub>		30		ns	R <sub>G</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		24		nC	I <sub>D</sub> = 20 A
Gate to Source Charge	Q <sub>GS</sub>		3.0		nC	V <sub>DD</sub> = 48 V
Gate to Drain Charge	Q <sub>GD</sub>		6.0		nC	V <sub>GS</sub> = 10 V
Body Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		95		ns	I <sub>F</sub> = 10 A, V <sub>GS</sub> = 0
Reverse Recovery Charge	Q <sub>rr</sub>		250		nC	di/dt = 100 A/μs

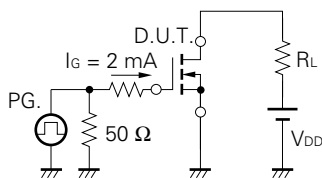
**Test Circuit 1 Avalanche Capability**



**Test Circuit 2 Switching Time**

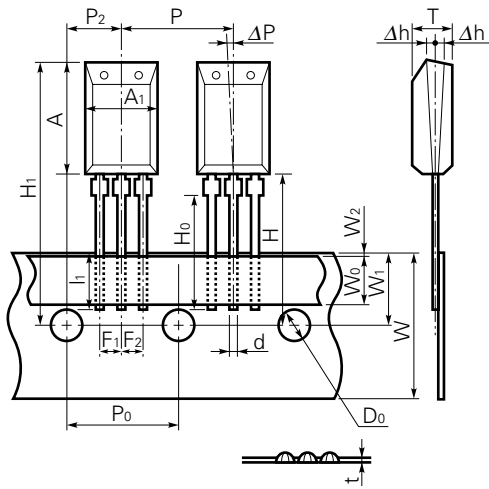


**Test Circuit 3 Gate Charge**



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

Radial Tape Specification

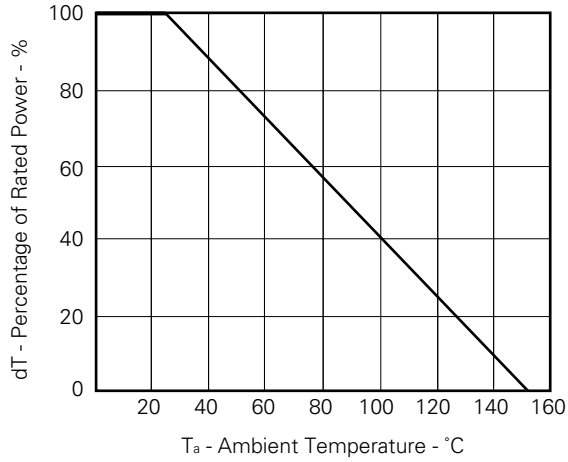


Dimension (unit: mm)

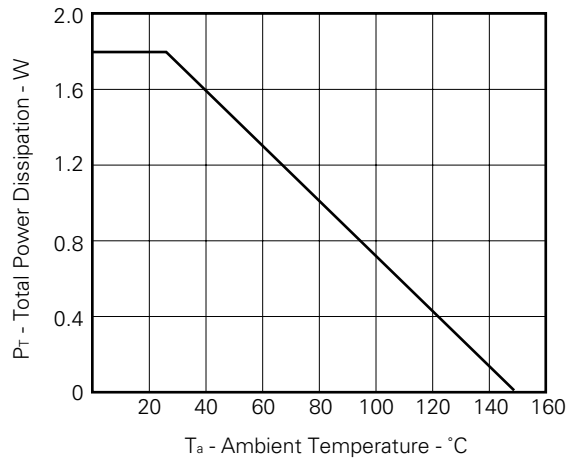
Item		
Component Body Length along Tape	$A_1$	$8.0 \pm 0.2$
Component Body Height	$A$	$13.0 \pm 0.2$
Component Body Width	$T$	$4.5 \pm 0.2$
Component Lead Width Dimension	$d$	$0.5 \pm 0.1$
Lead Wire Enclosure	$l_1$	2.5 MIN.
Component Center Pitch	$P$	$12.7 \pm 1.0$
Feedhole Pitch	$P_0$	$12.7 \pm 0.3$
Feedhole Center to Center Lead	$P_2$	$6.35 \pm 0.5$
Component Lead Pitch	$F_1, F_2$	$2.5 \begin{matrix} +0.4 \\ -0.1 \end{matrix}$
Deflection Front or Rear	$\Delta h$	$\pm 1.0$
Deflection Left or Right	$\Delta P$	$\pm 1.3$
Carrier Strip Width	$W$	$18.0 \begin{matrix} +1.0 \\ -0.5 \end{matrix}$
Adhesive Tape Width	$W_0$	5.0 MIN.
Feedhole Location	$W_1$	$9.0 \pm 0.5$
Adhesive Tape Position	$W_2$	0.7 MIN.
Height of Seating Plane	$H_0$	$16.0 \pm 0.5$
Feedhole to upper of Component	$H_1$	32.2 MAX.
Feedhole to Bottom of Component	$H$	20.0 MAX.
Tape Feedhole Diameter	$D_0$	$4.0 \pm 0.2$
Overall Taped Package Thickness	$t$	$0.7 \pm 0.2$

TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C)

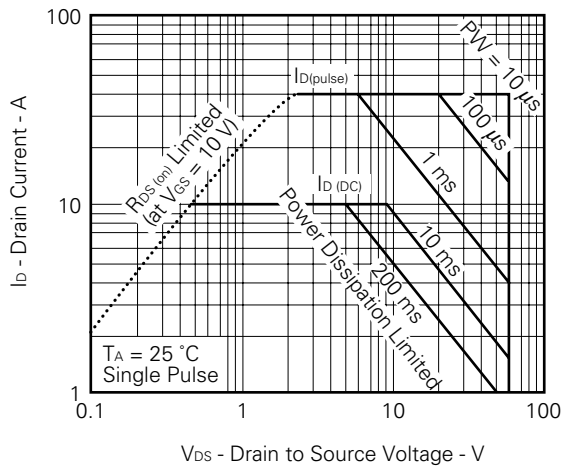
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



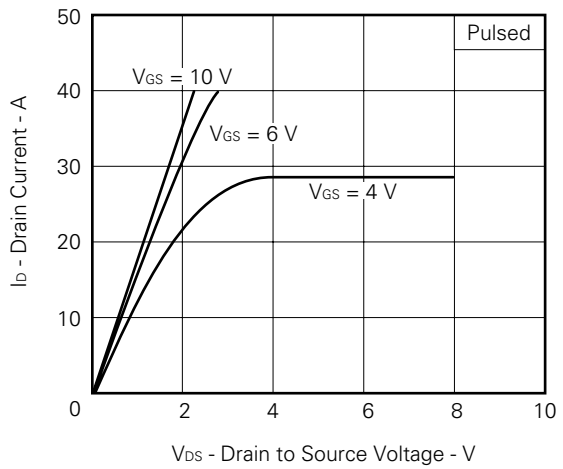
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



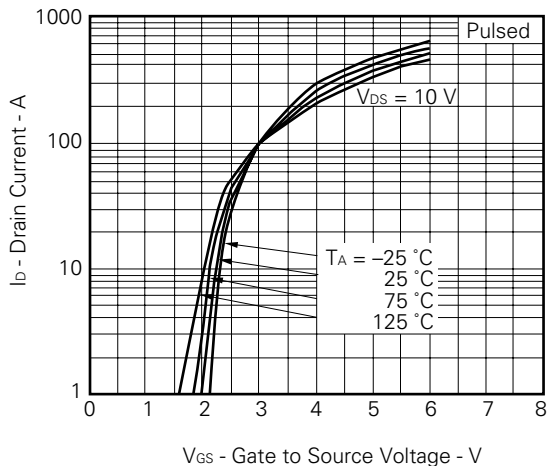
FORWARD BIAS SAFE OPERATING AREA



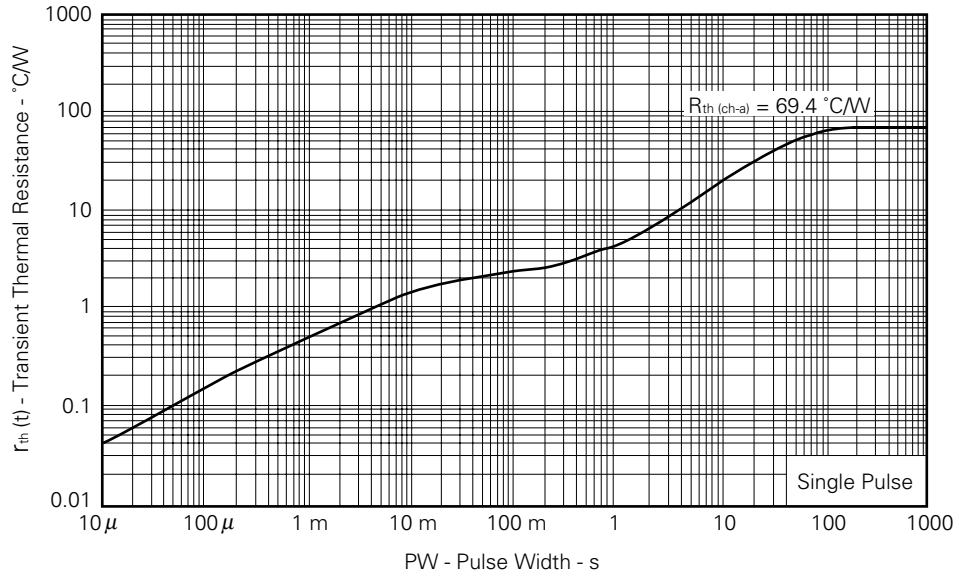
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



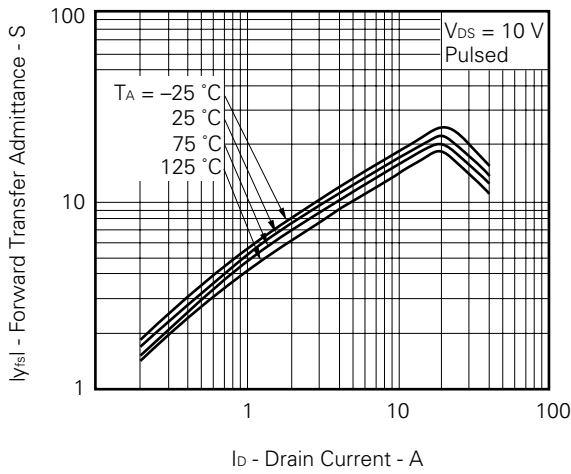
FORWARD TRANSFER CHARACTERISTICS



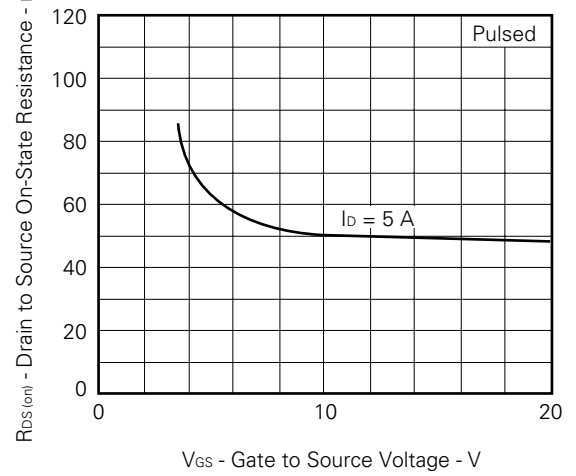
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



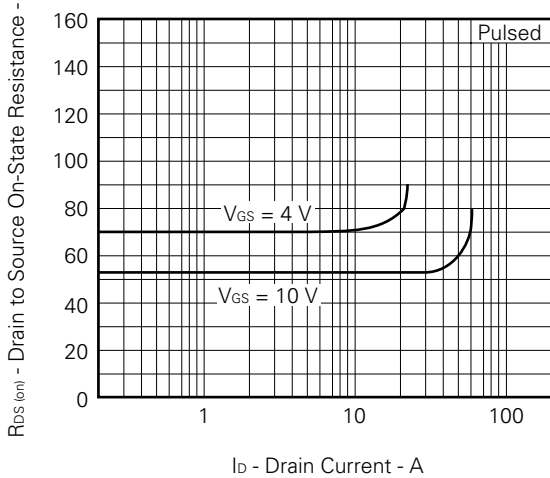
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



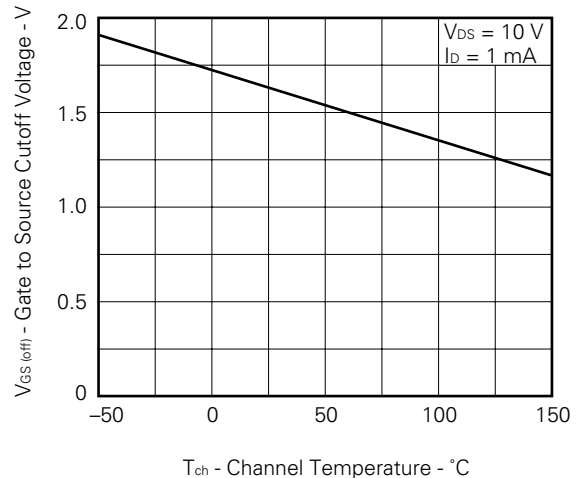
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



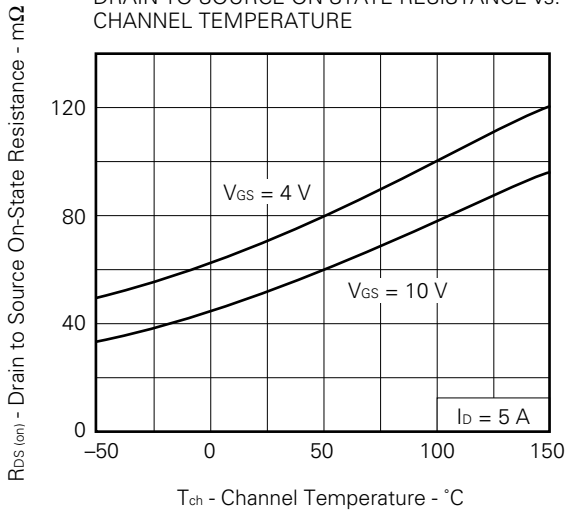
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



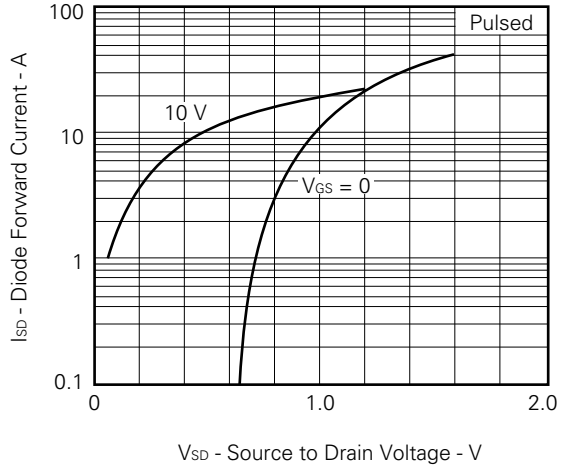
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



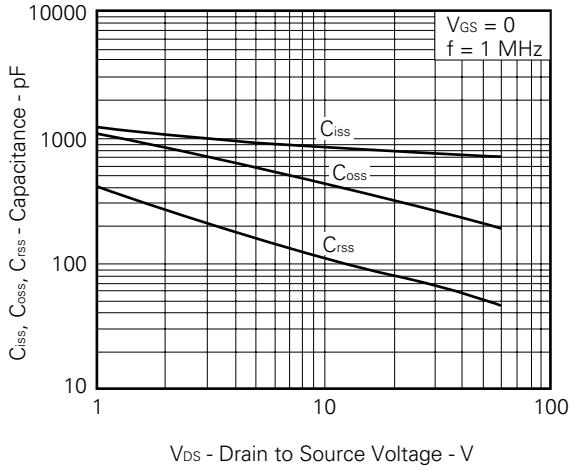
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



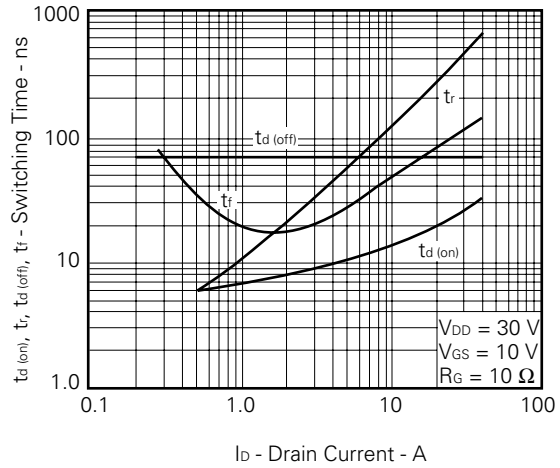
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



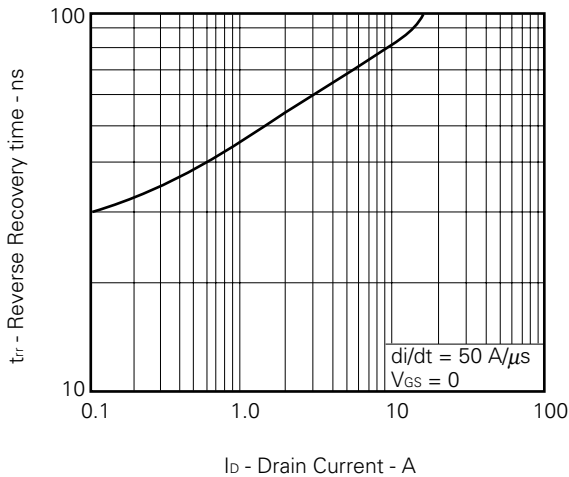
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



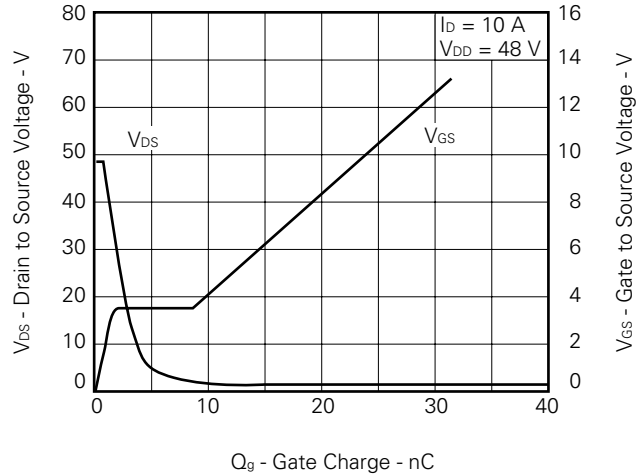
SWITCHING CHARACTERISTICS



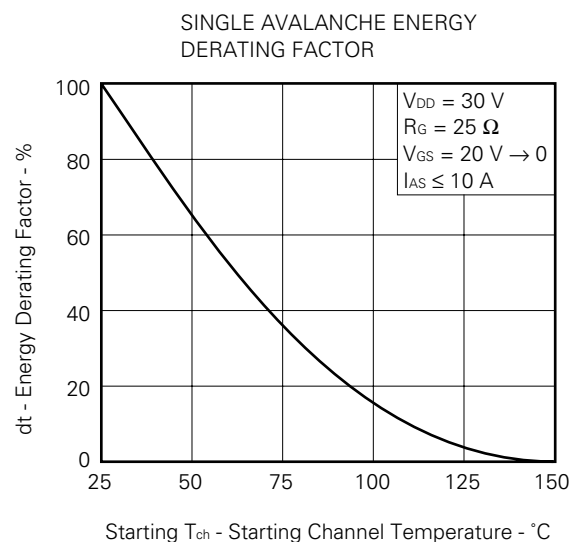
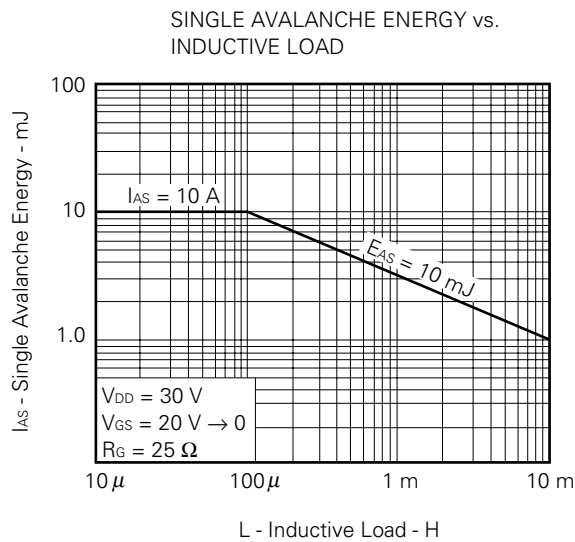
REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS







**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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