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P1 98.2

# MOS FIELD EFFECT POWER TRANSISTORS 2SK2136, 2SK2136-Z

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

### DESCRIPTION

The 2SK2136, 2SK2136-Z are N-channel Power MOS Field Effect Transistors designed for high voltage switching applications.

### FEATURES

- Low On-state Resistance  
 $R_{D(on)} = 0.18 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 10 \text{ A)}$
- Low  $C_{iss}$   $C_{iss} = 1100 \text{ pF TYP.}$
- High Avalanche Capability Ratings

### QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

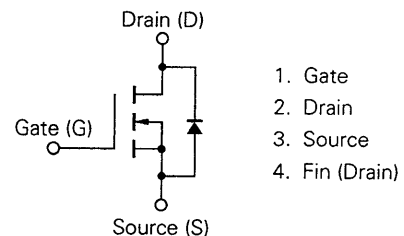
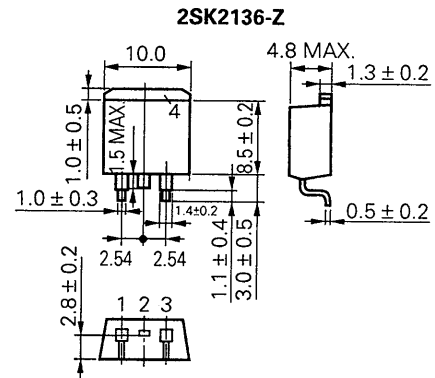
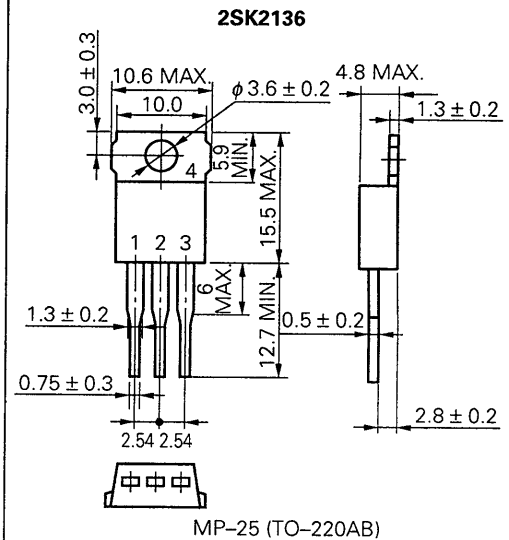
### ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DSS}$	200	V
Gate to Source Voltage	$V_{GSS}$	$\pm 30$	V
Drain Current (DC)	$I_{D(DS)}$	$\pm 20$	A
Drain Current (pulse)	$I_{D(pulse)^*}$	$\pm 80$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_{T1}$	75	W
Total Power Dissipation ( $T_a = 25^\circ\text{C}$ )	$P_{T2}$	1.5	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current	$I_{AS}^{**}$	20	A
Single Avalanche Energy	$E_{AS}^{**}$	80	mJ

\*  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

\*\* Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

### PACKAGE DIMENSIONS (Unit: mm)

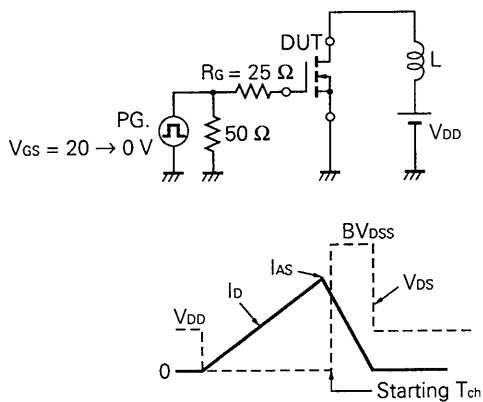


(Diode in the figure is the parasitic diode)

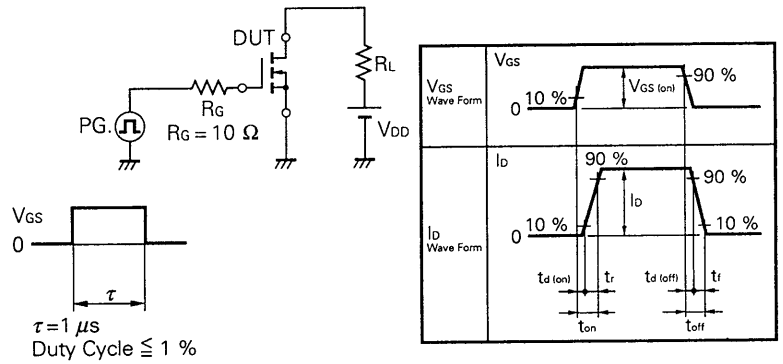
**ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 °C)**

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R <sub>DS(on)</sub>			0.18	Ω	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A
Gate to Source Cutoff Voltage	V <sub>GS(off)</sub>	2.0		4.0	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance	y <sub>fs</sub>	4.0			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 10 A
Drain Leakage Current	I <sub>DSS</sub>			100	μA	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0
Gate to Source Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0
Input Capacitance	C <sub>iss</sub>		1 100		pF	V <sub>DS</sub> = 10 V
Output Capacitance	C <sub>oss</sub>		540		pF	V <sub>GS</sub> = 0
Reverse Transfer Capacitance	C <sub>rss</sub>		190		pF	f = 1 MHz
Turn-On Delay Time	t <sub>d(on)</sub>		20		ns	V <sub>GS</sub> = 10 V
Rise Time	t <sub>r</sub>		85		ns	V <sub>DD</sub> = 100 V
Turn-Off Delay Time	t <sub>d(off)</sub>		60		ns	I <sub>D</sub> = 10 A, R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		25		ns	R <sub>L</sub> = 10 Ω
Total Gate Charge	Q <sub>G</sub>		30		nC	V <sub>GS</sub> = 10 V
Gate to Source Charge	Q <sub>GS</sub>		7.0		nC	I <sub>D</sub> = 20 A
Gate to Drain Charge	Q <sub>GD</sub>		15		nC	V <sub>DD</sub> = 160 V
Diode Forward Voltage	V <sub>F(S-D)</sub>		1.0		V	I <sub>F</sub> = 20 A, V <sub>GS</sub> = 0
Reverse Recovery Time	t <sub>rr</sub>		210		ns	I <sub>F</sub> = 20 A
Reverse Recovery Charge	Q <sub>rr</sub>		1.0		μC	di/dt = 50 A/μs

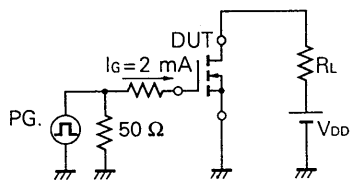
**Test Circuit 1 : Avalanche Capability**



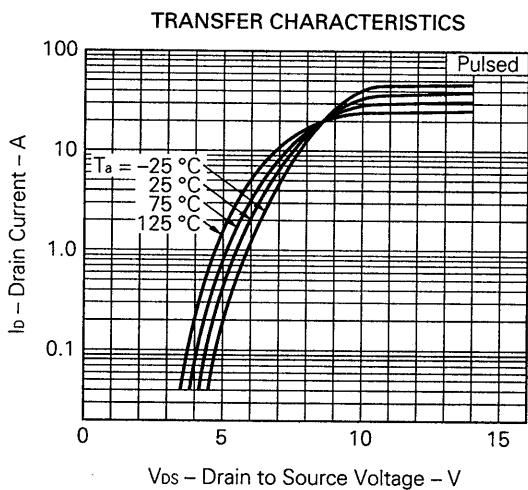
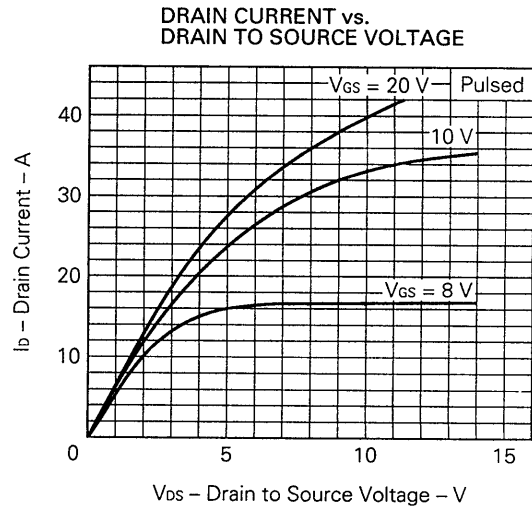
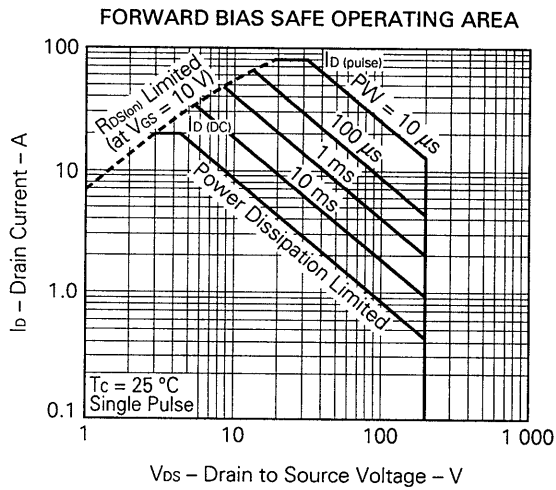
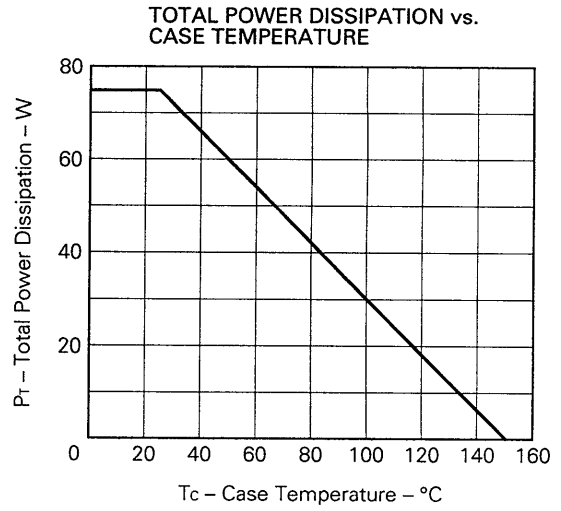
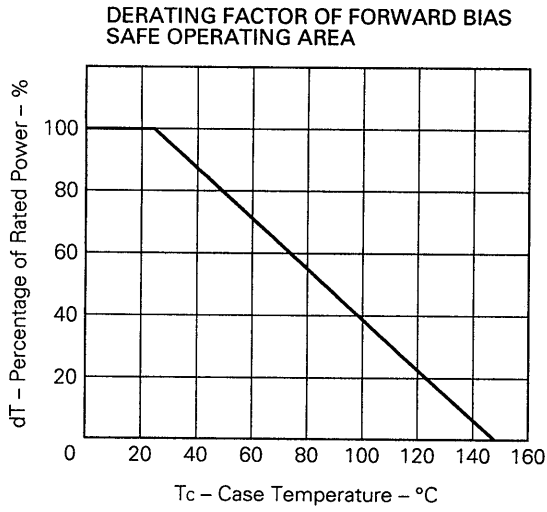
**Test Circuit 2 : Switching Time**



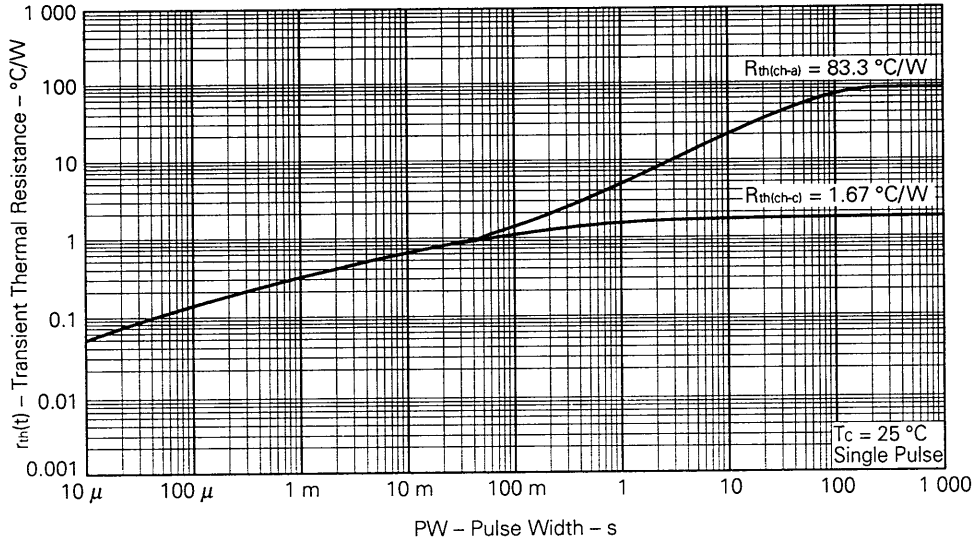
**Test Circuit 3 : Gate Charge**



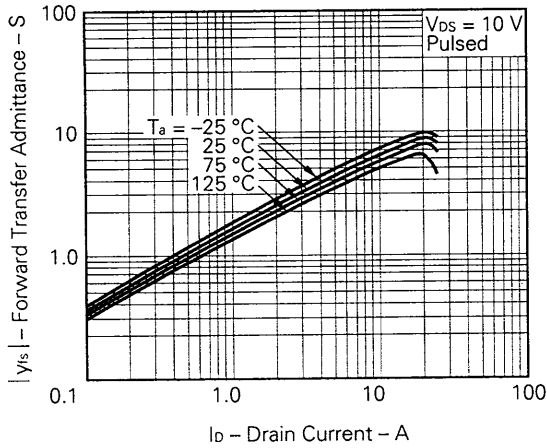
TYPICAL CHARACTERISTICS ( $T_a = 25\text{ }^\circ\text{C}$ )



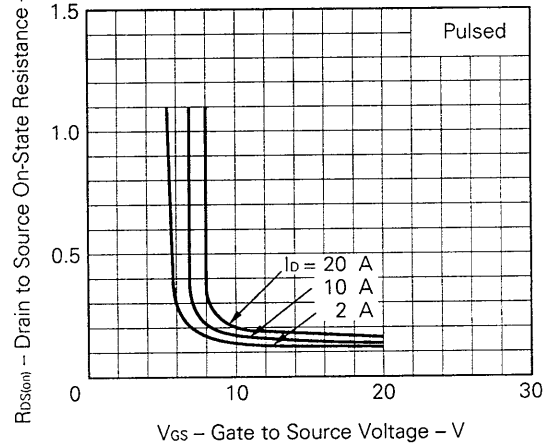
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



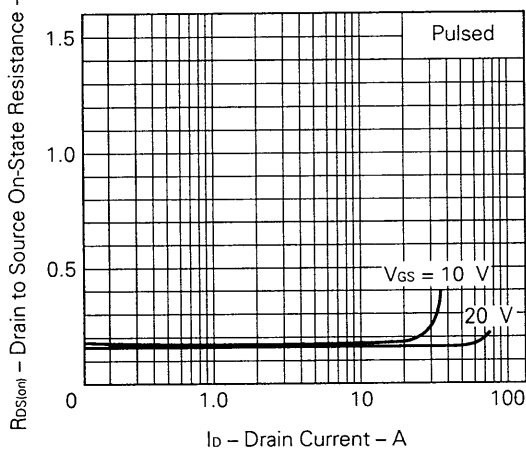
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



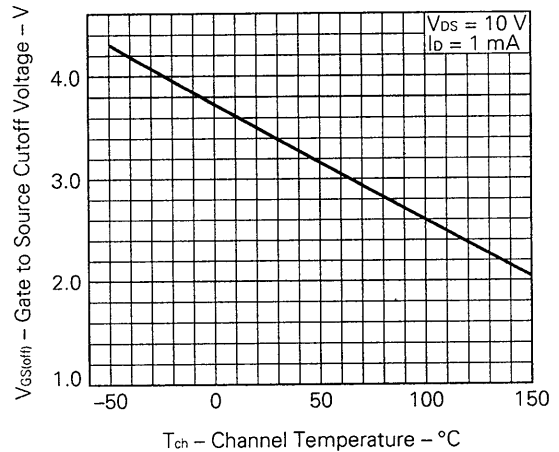
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



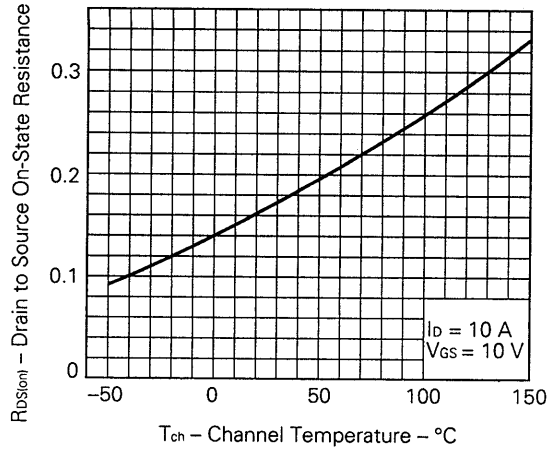
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



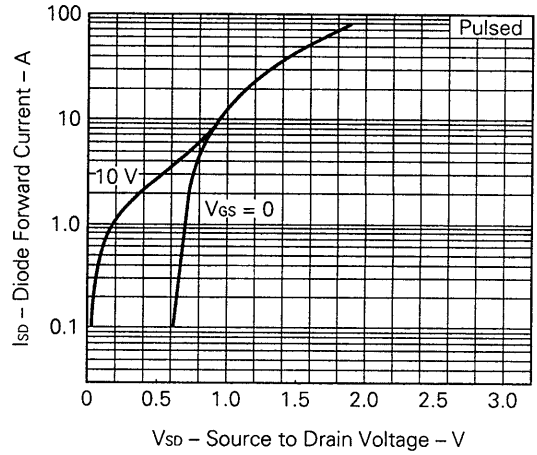
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



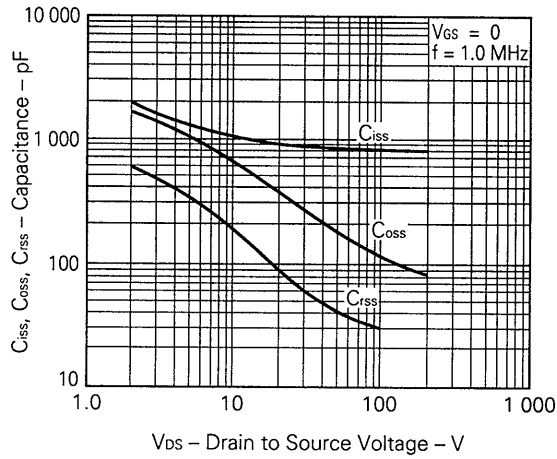
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



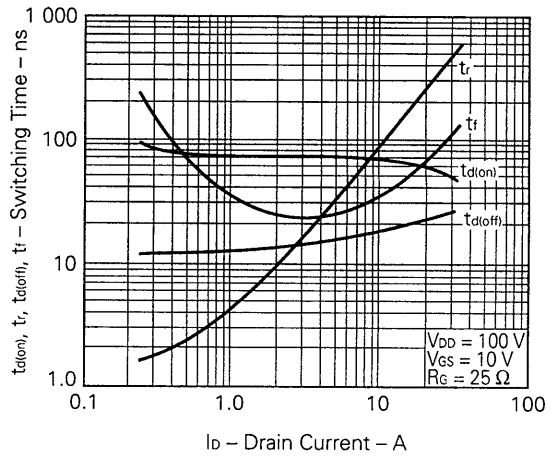
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



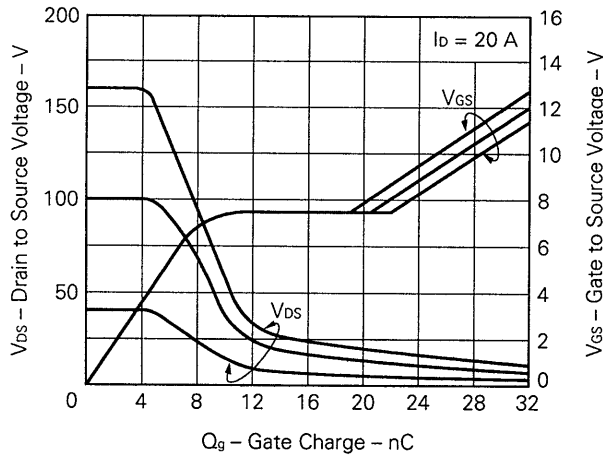
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



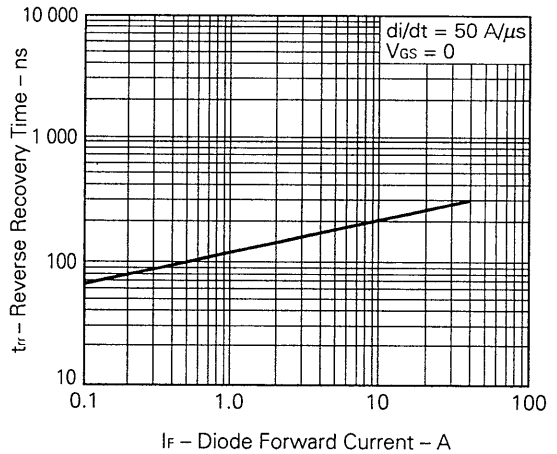
SWITCHING CHARACTERISTICS



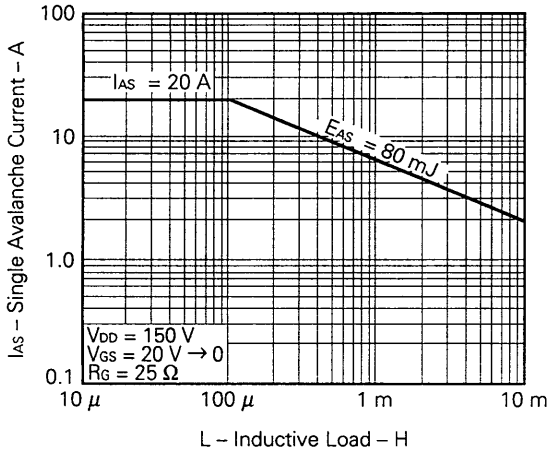
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



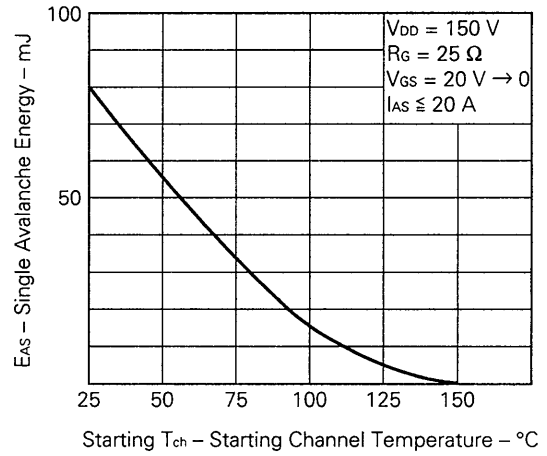
REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs. STARTING CHANNEL TEMPERATURE



[MEMO]



**Reference**

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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