

MOS FIELD EFFECT POWER TRANSISTOR
2SK2135

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2135 is N-channel Power MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} = 0.18 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 7.0 \text{ A)}$
- Low C_{iss} $C_{iss} = 1 \text{ } 100 \text{ pF TYP.}$
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

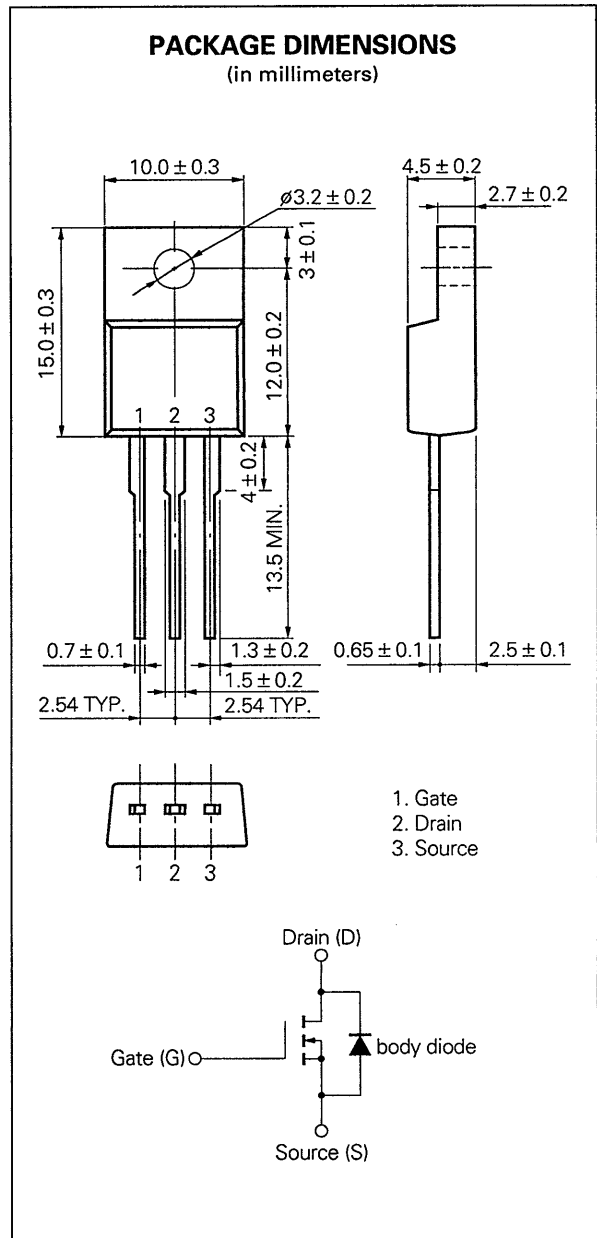
ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

| | | | |
|--|------------------------|-------------|----|
| Drain to Source Voltage | V _{DSS} | 200 | V |
| Gate to Source Voltage | V _{GSS} | ±30 | V |
| Drain Current (DC) | I _{D(DC)} | ±14 | A |
| Drain Current (pulse) | I _{D(pulse)*} | ±56 | A |
| Single Avalanche Current | I _{AS**} | 14 | A |
| Single Avalanche Energy | E _{AS**} | 392 | mJ |
| Total Power Dissipation (T _c = 25 °C) | P _{T1} | 35 | W |
| Total Power Dissipation (T _a = 25 °C) | P _{T2} | 2.0 | W |
| Storage Temperature | T _{stg} | -55 to +150 | °C |
| Channel Temperature | T _{ch} | 150 | °C |

* PW ≤ 10 μs, Duty Cycle ≤ 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

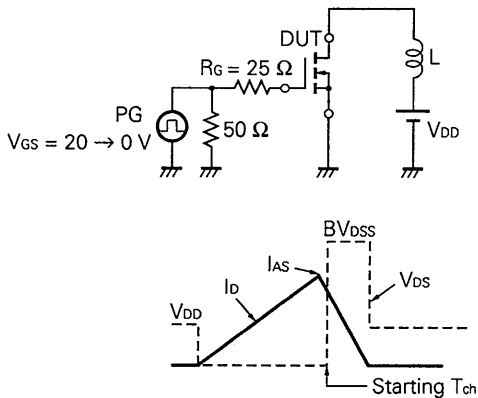
PACKAGE DIMENSIONS
 (in millimeters)



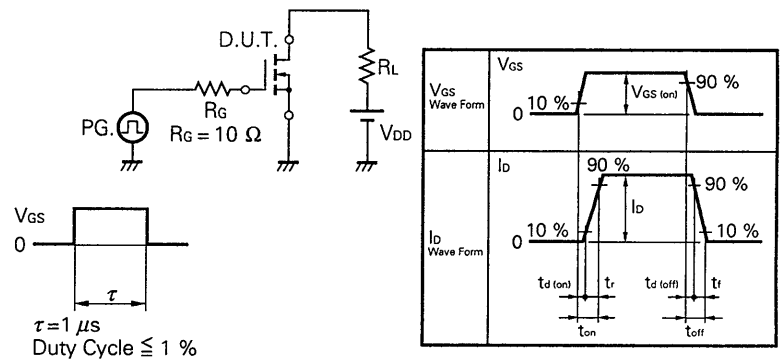
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|-------------------------------------|----------------------|------|-------|------|------|---|
| Drain to Source On-state Resistance | R _{DS(on)} | | | 0.18 | Ω | V _{GS} = 10 V, I _D = 7 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | 2.0 | | 4.0 | V | V _{DS} = 10 V, I _b = 1 mA |
| Forward Transfer Admittance | y _{fs} | 4.0 | | | S | V _{DS} = 10 V, I _D = 7 A |
| Drain Leakage Current | I _{DSS} | | | 100 | μA | V _{DS} = 200 V, V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±100 | nA | V _{GS} = ±30 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 1 100 | | pF | V _{DS} = 10 V V _{GS} = 0 f = 1 MHz |
| Output Capacitance | C _{oss} | | 540 | | pF | |
| Reverse Transfer Capacitance | C _{rss} | | 190 | | pF | |
| Turn-On Delay Time | t _{d(on)} | | 20 | | ns | V _{GS} = 10 V V _{DD} = 100 V I _D = 7 A, R _G = 10 Ω R _L = 14.3 Ω |
| Rise Time | t _r | | 50 | | ns | |
| Turn-Off Delay Time | t _{d(off)} | | 65 | | ns | |
| Fall Time | t _f | | 25 | | ns | |
| Total Gate Charge | Q _G | | 30 | | nC | V _{GS} = 10 V I _D = 14 A V _{DD} = 160 V |
| Gate to Source Charge | Q _{GS} | | 7.0 | | nC | |
| Gate to Drain Charge | Q _{GD} | | 15 | | nC | |
| Diode Forward Voltage | V _{F(S-D)} | | 1.0 | | V | I _F = 14 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 170 | | ns | I _F = 14 A di/dt = 50 A/μs |
| Reverse Recovery Charge | Q _{rr} | | 0.6 | | μC | |

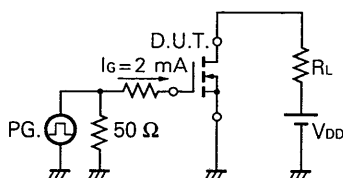
Test Circuit 1 : Avalanche Capability



Test Circuit 2 : Switching Time

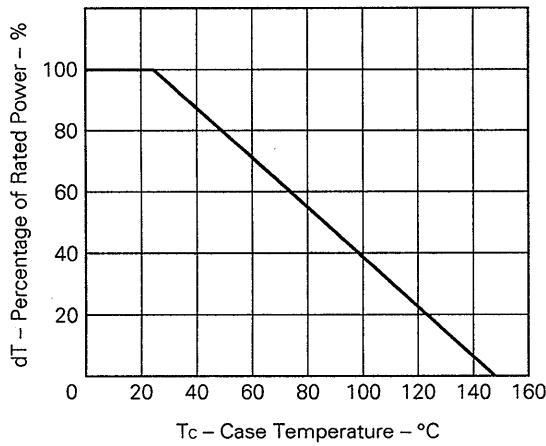


Test Circuit 3 : Gate Charge

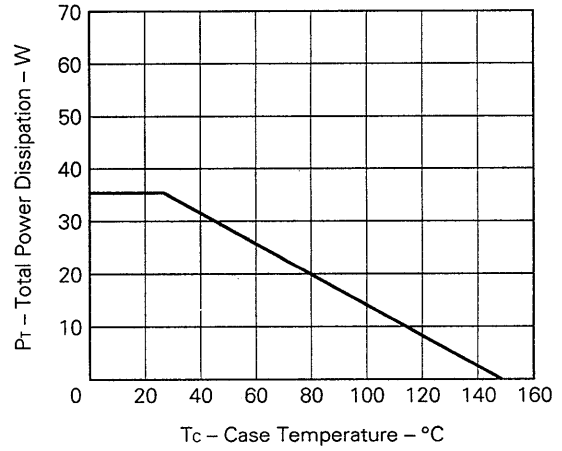


TYPICAL CHARACTERISTICS ($T_a = 25\text{ }^\circ\text{C}$)

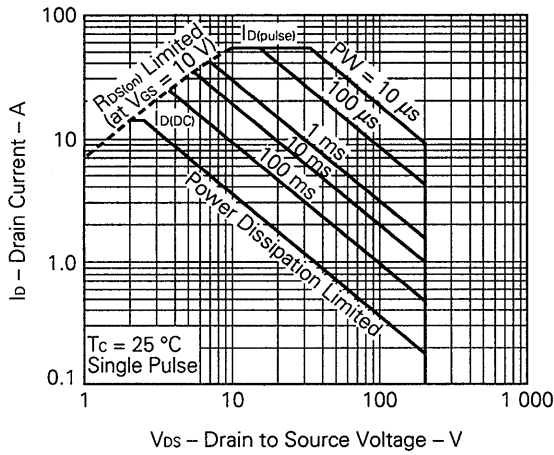
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



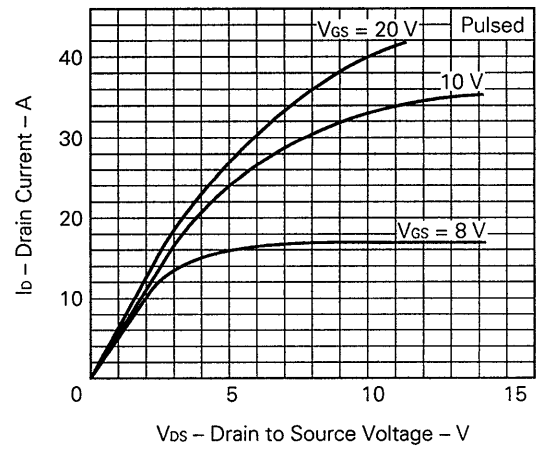
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



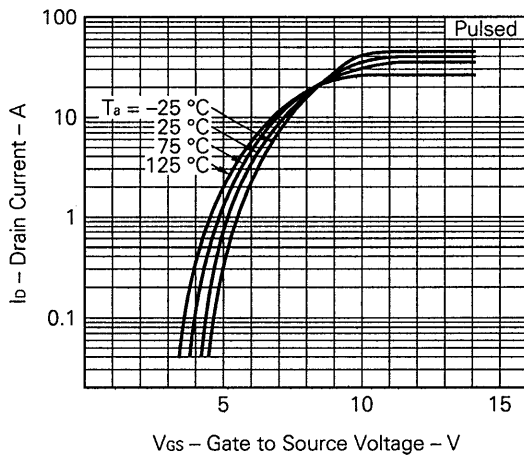
FORWARD BIAS SAFE OPERATING AREA

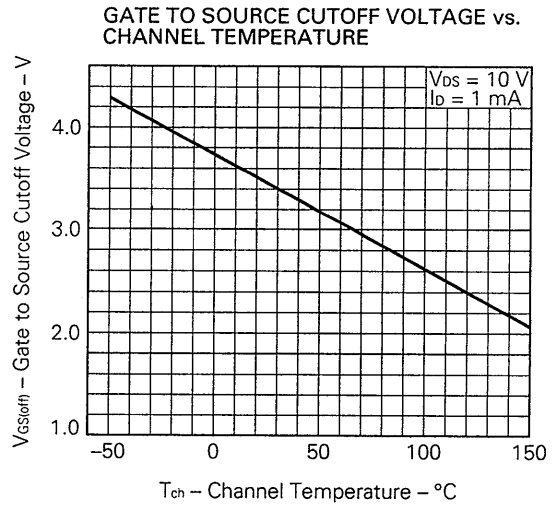
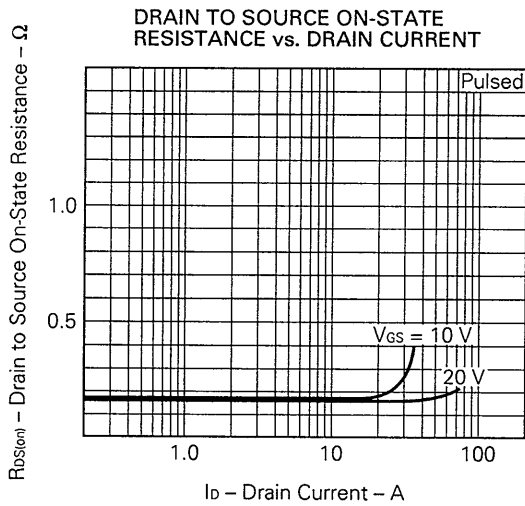
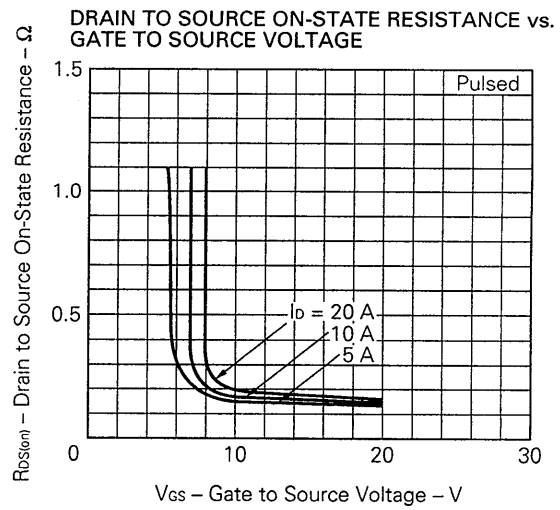
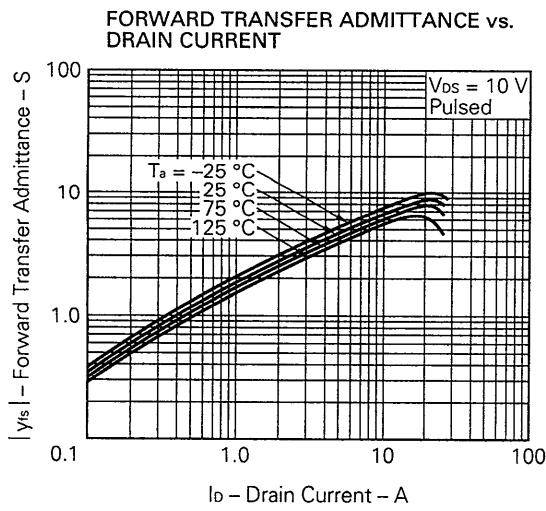
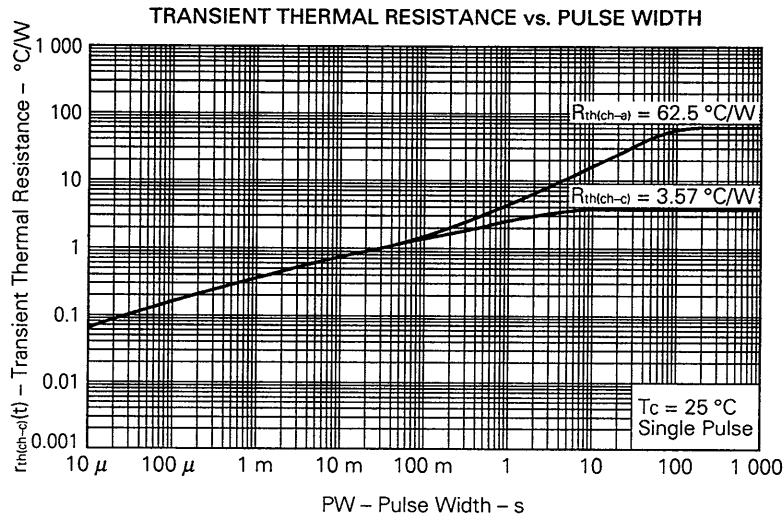


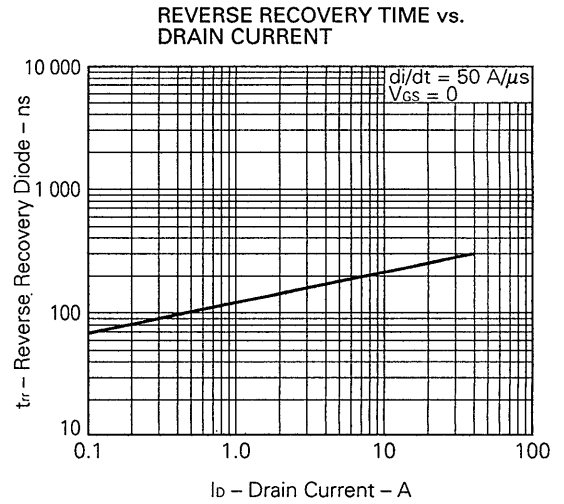
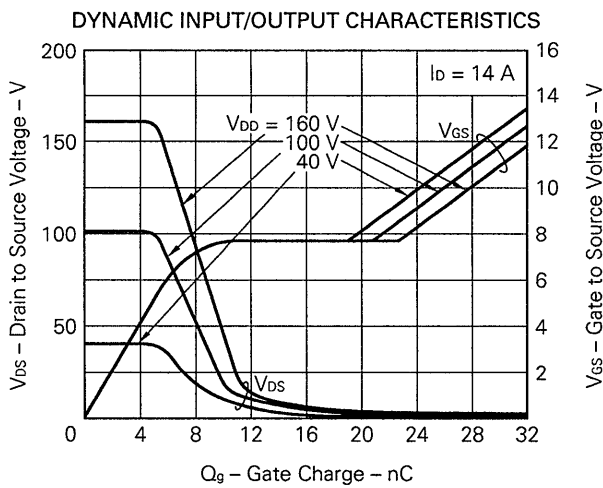
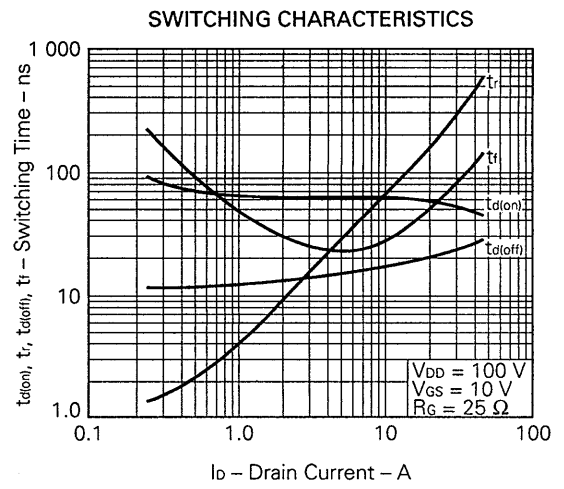
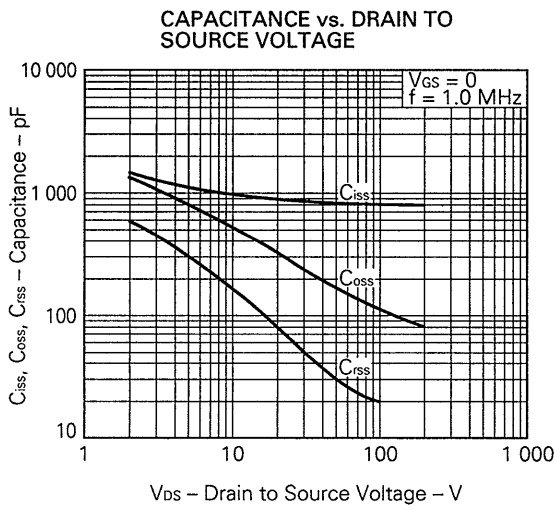
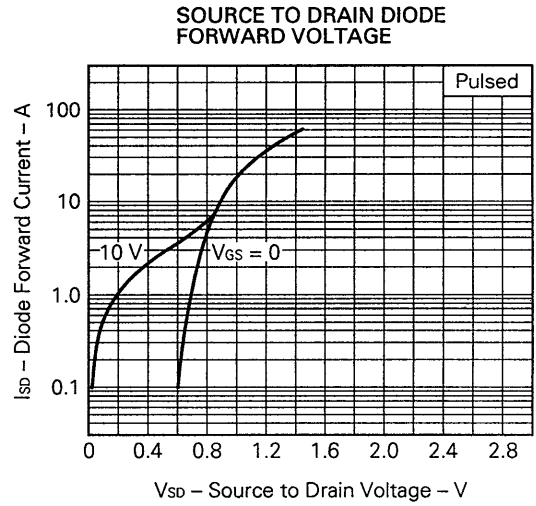
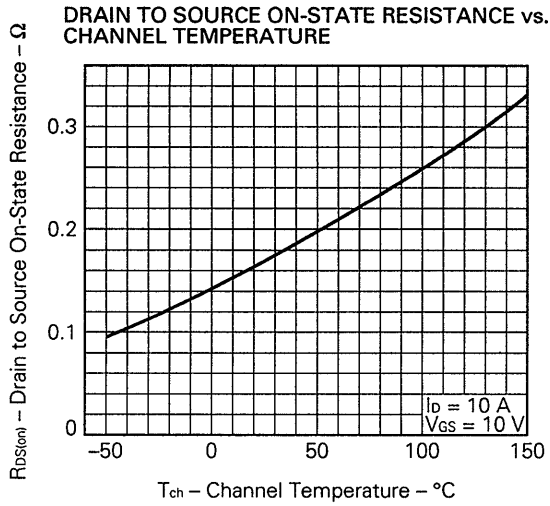
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

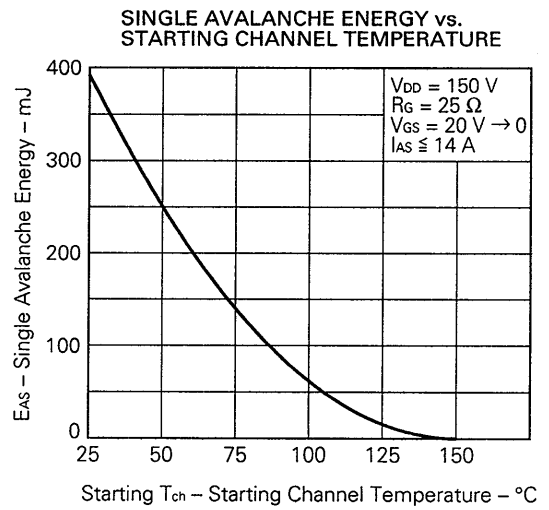
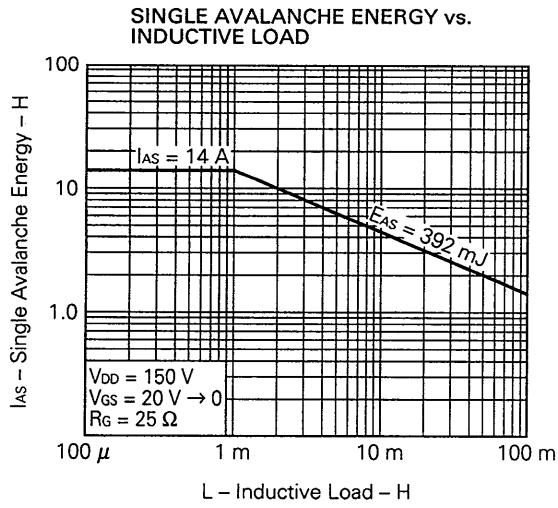


SOURCE TO DRAIN DIODE FORWARD VOLTAGE









[MEMO]

Reference

| Application note name | No. |
|--|----------|
| Safe operating area of Power MOS FET. | TEA-1034 |
| Application circuit using Power MOS FET. | TEA-1035 |
| Quality control of NEC semiconductors devices. | TEI-1202 |
| Quality control guide of semiconductors devices. | MEI-1202 |
| Assembly manual of semiconductors devices. | IEI-1207 |

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