

MOS FIELD EFFECT POWER TRANSISTOR

2SK1796

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

The 2SK1796 is N-channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
 $R_{DS(on)} \leq 1.2 \Omega$ ($V_{GS} = 10 V, I_D = 5 A$)
- Low C_{iss} $C_{iss} = 2\ 500$ pF TYP.
- Built-in G-S Gate Protection Diode
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

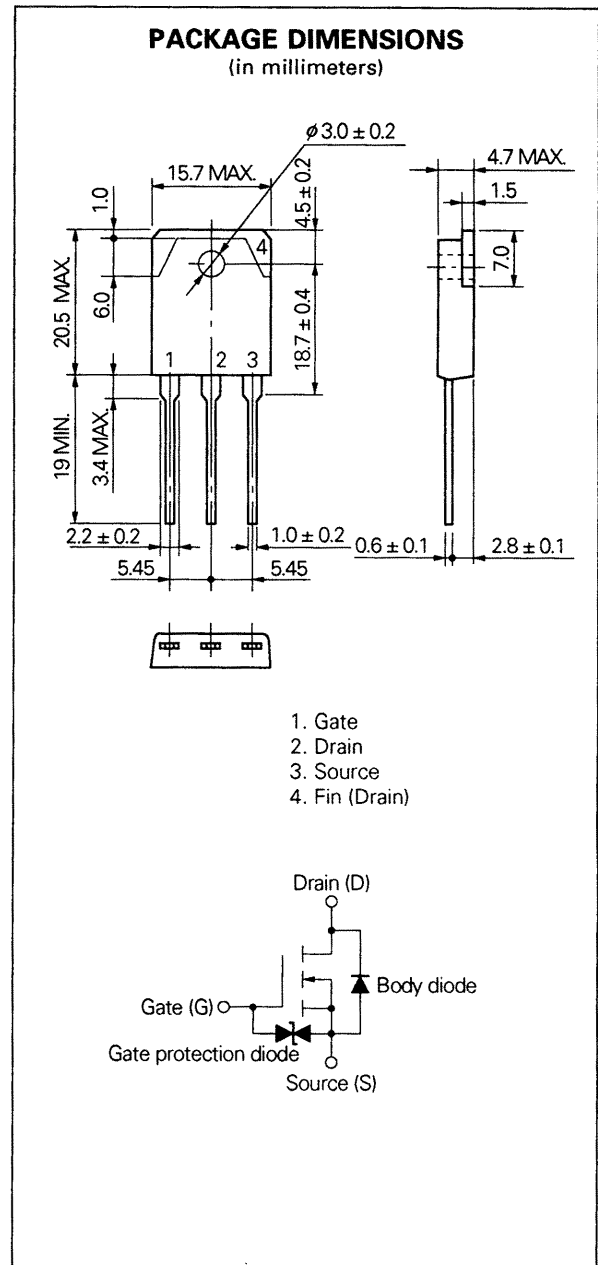
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS ($T_a = 25\ ^\circ C$)

Drain to Source Voltage	V_{DSS}	900	V
Gate to Source Voltage	V_{GSS}	± 30	V
Drain Current (DC)	$I_{D(DC)}$	± 10	A
Drain Current (pulse)	$I_{D(pulse)^*}$	± 20	A
Total Power Dissipation ($T_c = 25\ ^\circ C$)	P_T	150	W
Channel Temperature	T_{ch}	150	$^\circ C$
Storage Temperature	T_{stg}	-55 to +150	$^\circ C$
Single Avalanche Current	I_{AS}^{**}	10	A
Single Avalanche Energy	E_{AS}^{**}	60	mJ

* $PW \leq 10\ \mu s$, Duty Cycle $\leq 1\ %$

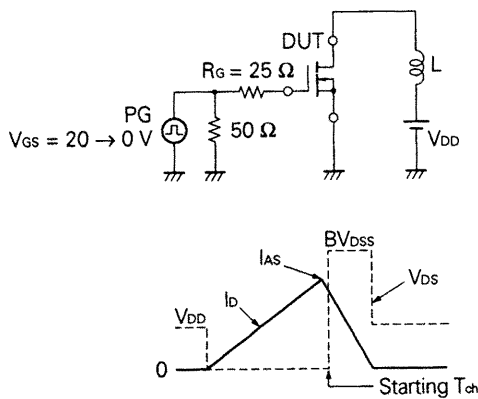
** Starting $T_{ch} = 25\ ^\circ C$, $R_G = 25\ \Omega$, $V_{GS} = 20\ V \rightarrow 0$



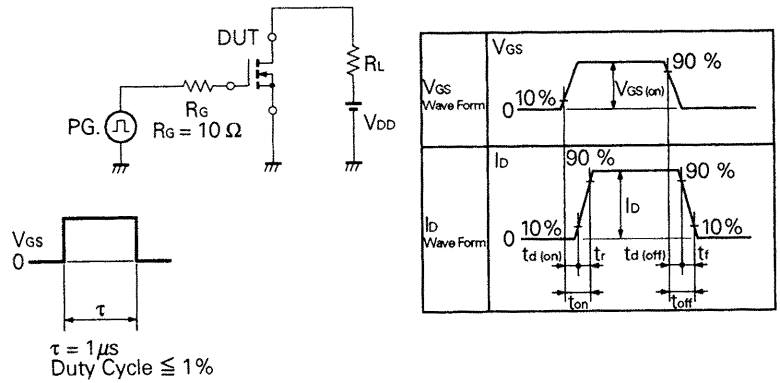
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		1.0	1.2	Ω	V _{GS} = 10 V, I _b = 5 A
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _b = 1 mA
Forward Transfer Admittance	y _{fs}	1.5	7.5		S	V _{DS} = 20 V, I _b = 5 A
Drain Leakage Current	I _{DSS}			100	μA	V _{DS} = 900 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±30 V, V _{DS} = 0
Input Capacitance	C _{iss}		2 500		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		370		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		120		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		40		ns	V _{GS(on)} = 10 V
Rise Time	t _r		50		ns	V _{DD} = 150 V
Turn-Off Delay Time	t _{d(off)}		190		ns	I _b = 5 A, R _G = 10 Ω
Fall Time	t _f		40		ns	R _L = 30 Ω
Total Gate Charge	Q _G		90		nC	V _{GS} = 10 V
Gate to Source Charge	Q _{GS}		18		nC	I _b = 10 A
Gate to Drain Charge	Q _{GD}		38		nC	V _{DD} = 720 V
Diode Forward Voltage	V _{F(S-D)}		0.9		V	I _F = 10 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		790		ns	I _F = 10 A
Reverse Recovery Charge	Q _{rr}		6.6		μC	di/dt = 50 A/μs

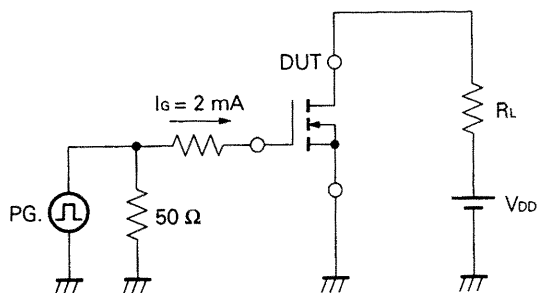
Test Circuit 1: Avalanche Capability



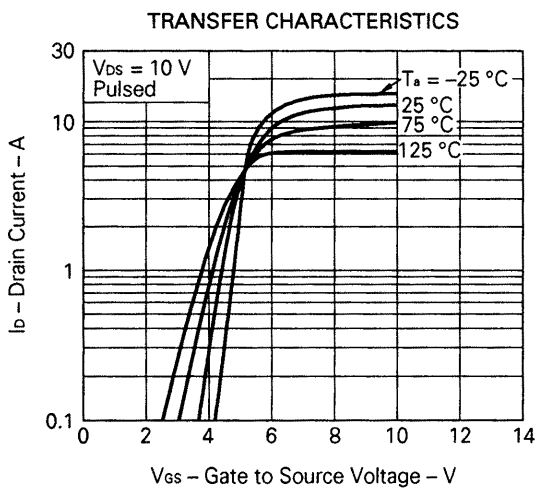
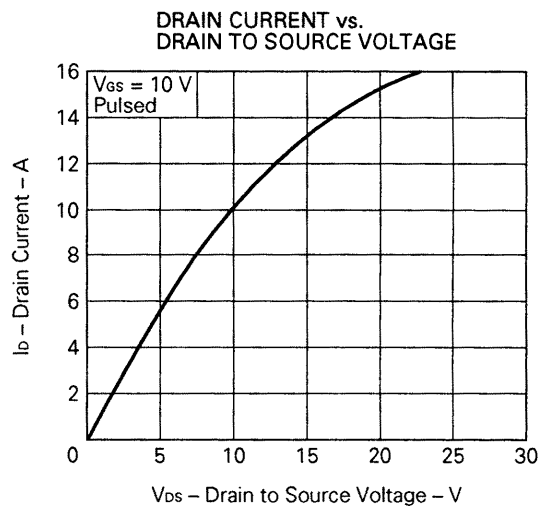
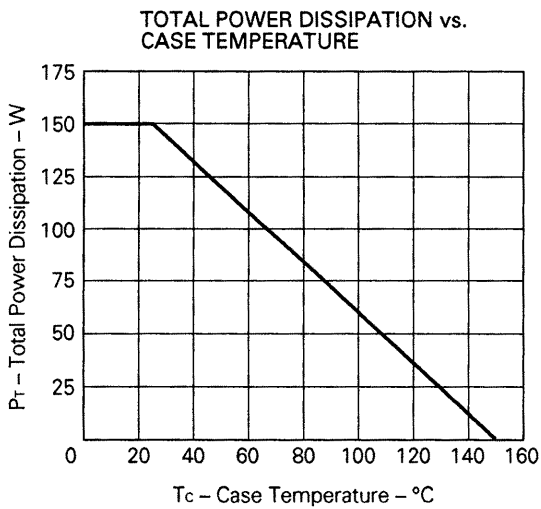
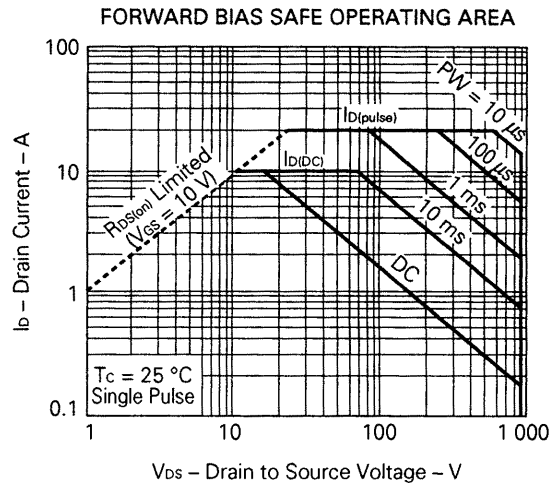
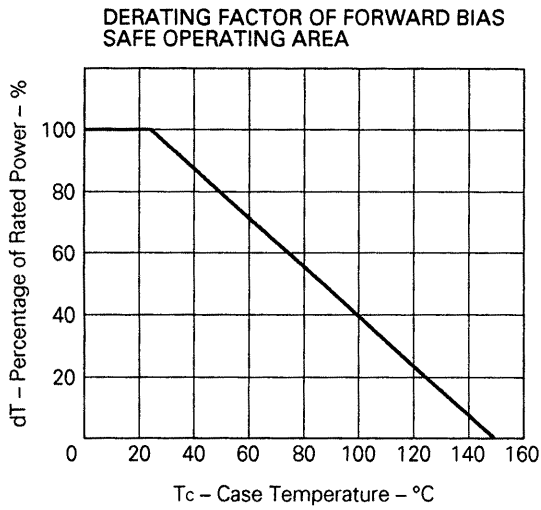
Test Circuit 2: Switching Time



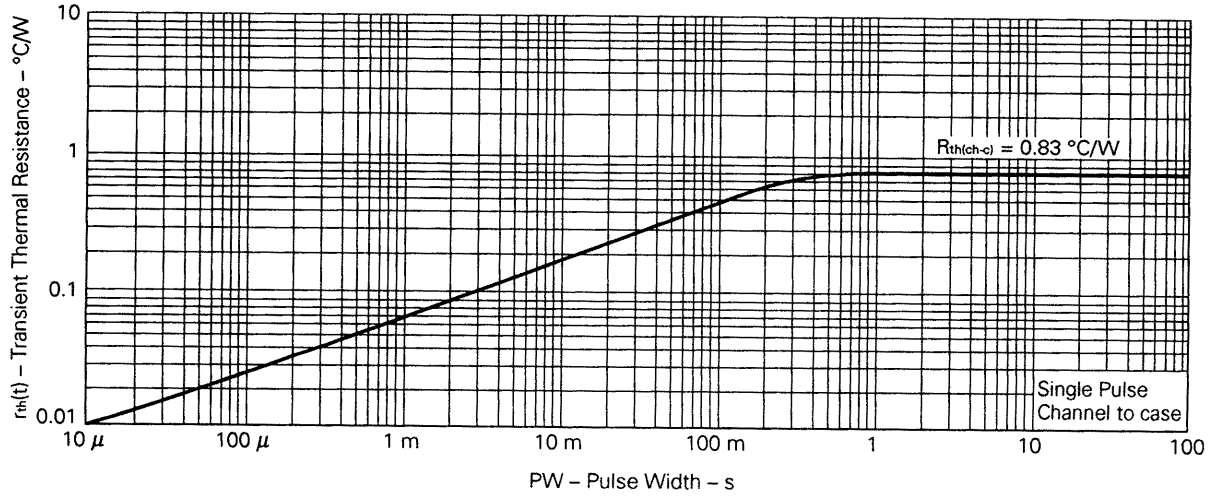
Test Circuit 3: Gate Charge



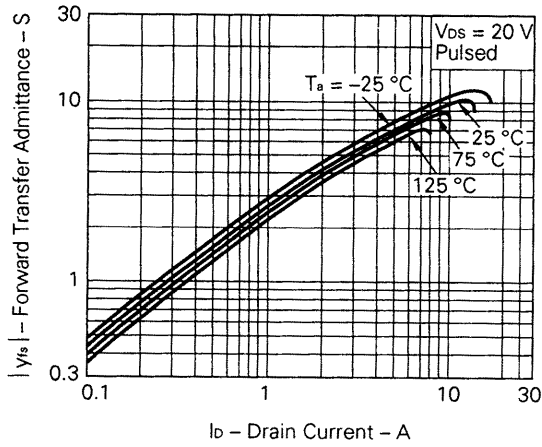
TYPICAL CHARACTERISTICS (T_a = 25 °C)



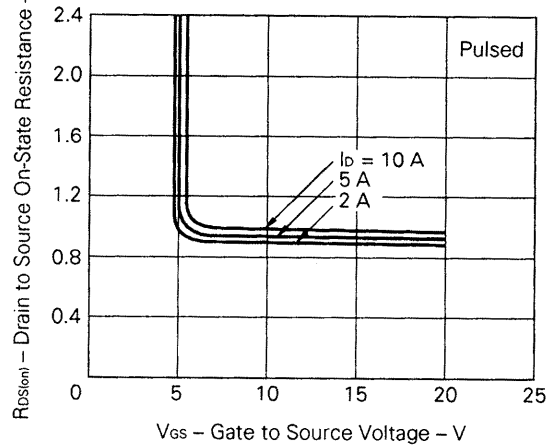
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



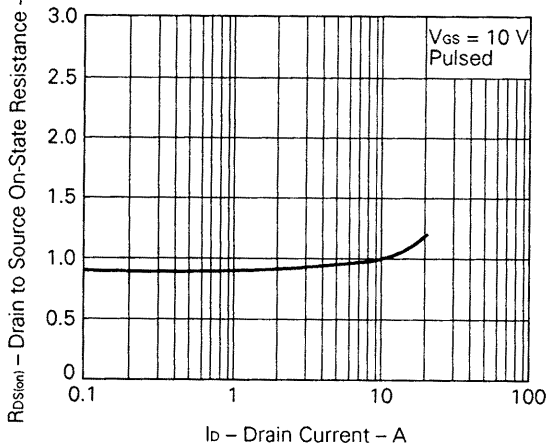
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



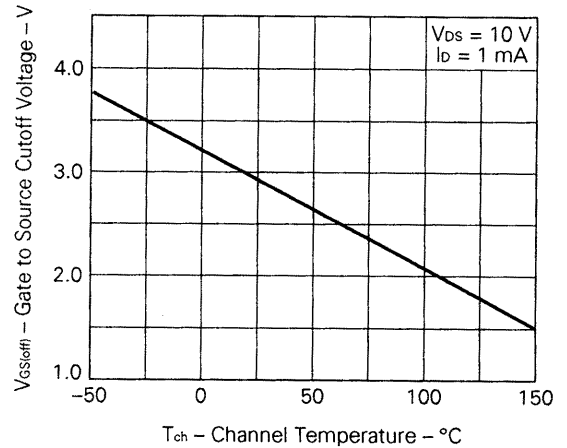
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

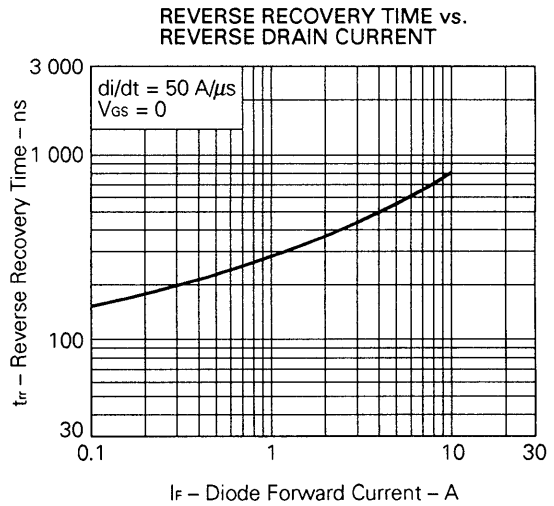
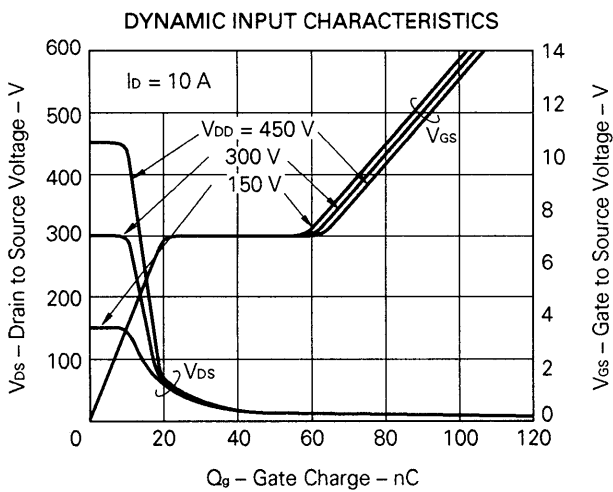
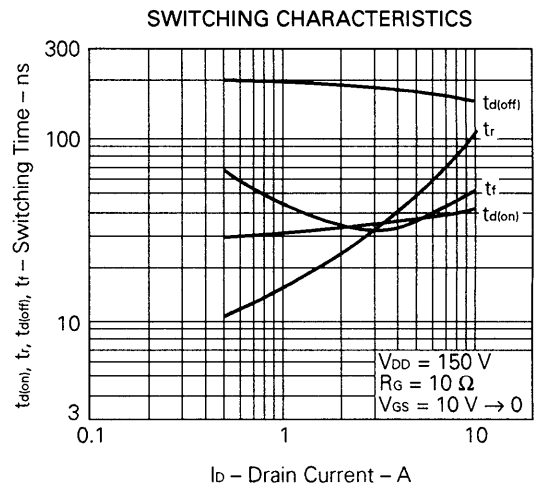
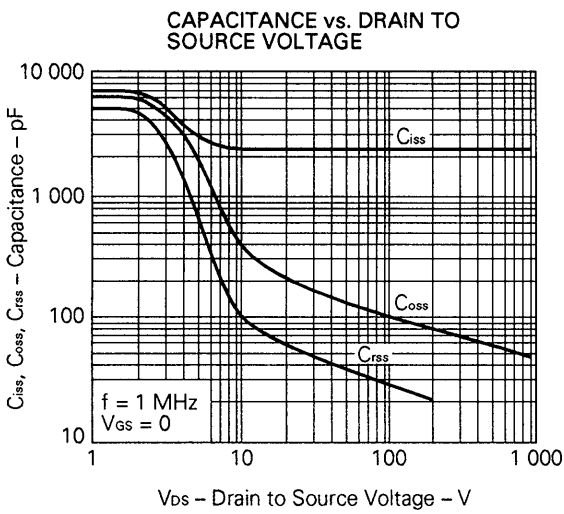
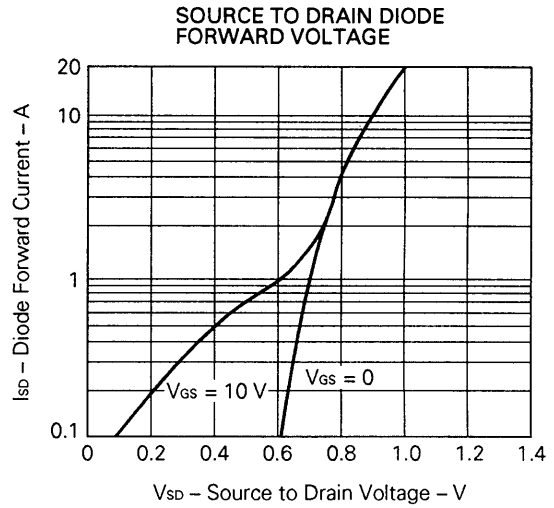
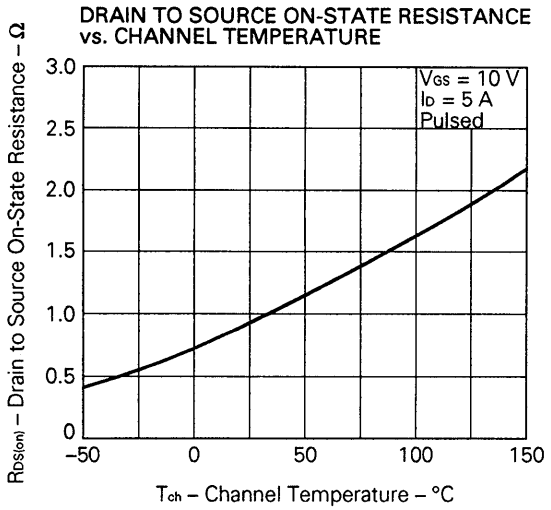


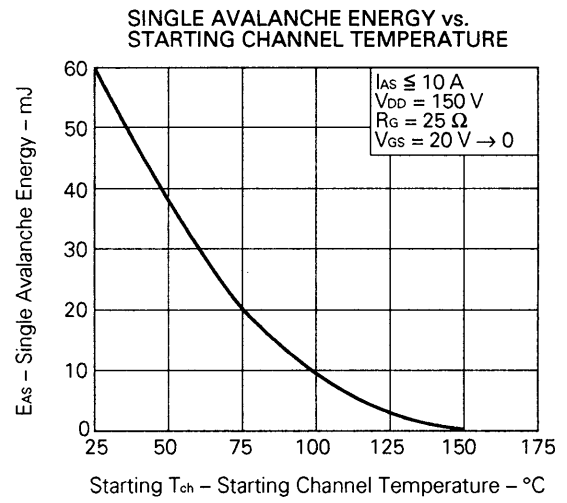
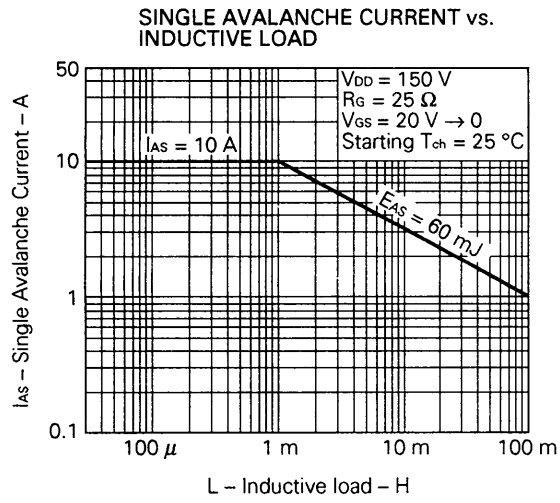
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE







Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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