To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

Phase-out/Discontinued

2SK1492

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK1492 is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

- Low on-state resistance
  $R_{DS(on)}$ = 0.1 Ω MAX. (V_{GS} = 10 V, I_D = 18 A)
- Low input capacitance C_{iss} = 3000 pF TYP.
- Built-in G-S gate protection diodes
- High avalanche capability ratings

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	250	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DC)}$	±35	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±140	A
Total Power Dissipation (T_C = 25°C)	P_T	140	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note2	I_{AS}	52.5	A
Single Avalanche Energy Note2	E_{AS}	2500	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 → 0 V

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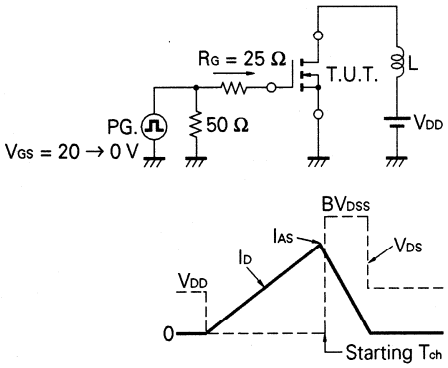
Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

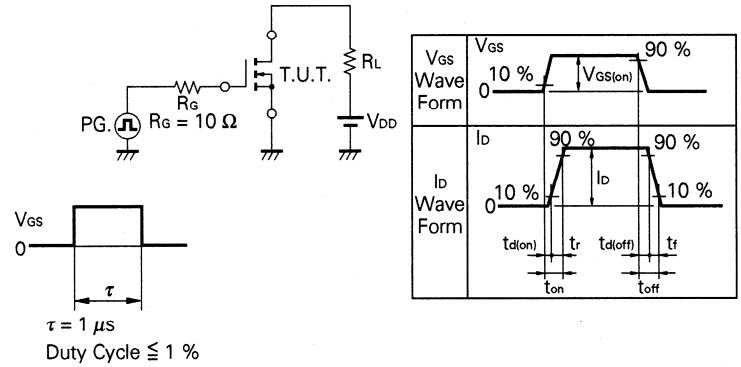
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$		0.08	0.1	Ω	V_{GS} = 10 V, I_D = 18 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.5		3.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	10			S	V_{DS} = 10 V, I_D = 18 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 250 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±10	μA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		3 000		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		1 500		pF	
Reverse Transfer Capacitance	C_{rss}		620		pF	
Turn-On Delay Time	$t_{d(on)}$		50		ns	V_{GS} = 10 V V_{DD} = 150 V I_D = 18 A, R_G = 10 Ω R_L = 8.3 Ω
Rise Time	t_r		240		ns	
Turn-Off Delay Time	$t_{d(off)}$		140		ns	
Fall Time	t_f		100		ns	
Total Gate Charge	Q_G		80		nC	V_{GS} = 10 V I_D = 35 A V_{DD} = 200 V
Gate to Source Charge	Q_{GS}		17		nC	
Gate to Drain Charge	Q_{GD}		50		nC	
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 35 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		370		ns	I_F = 35 A di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		2.8		μC	

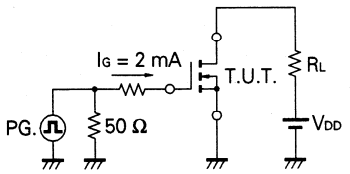
Test Circuit 1: Avalanche Time



Test Circuit 2: Switching Time

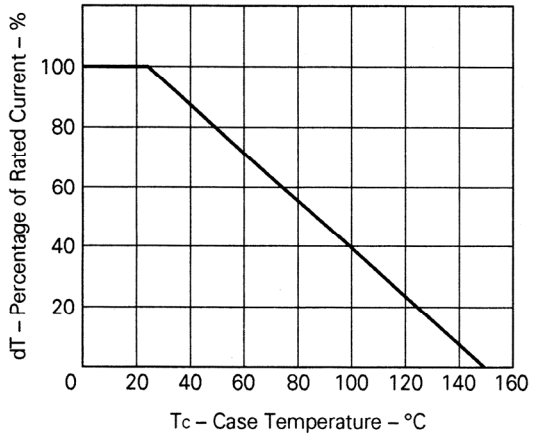


Test Circuit 3: Gate Charge

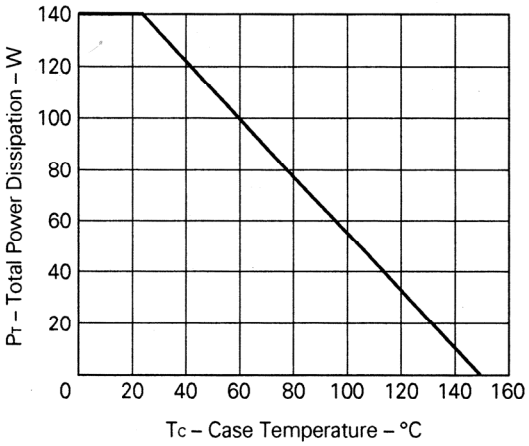


TYPICAL CHARACTERISTICS (T_a = 25 °C)

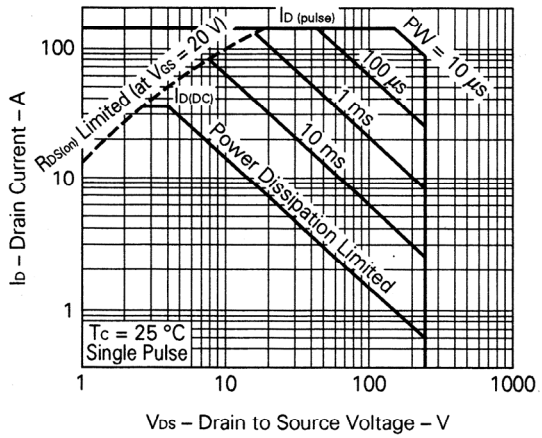
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



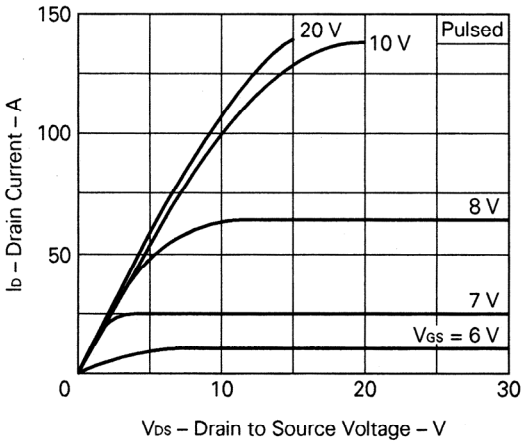
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



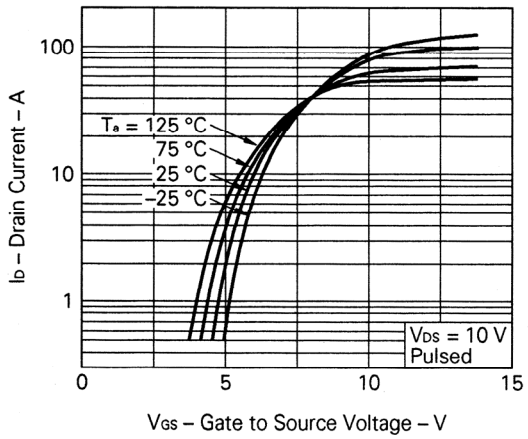
FORWARD BIAS SAFE OPERATING AREA



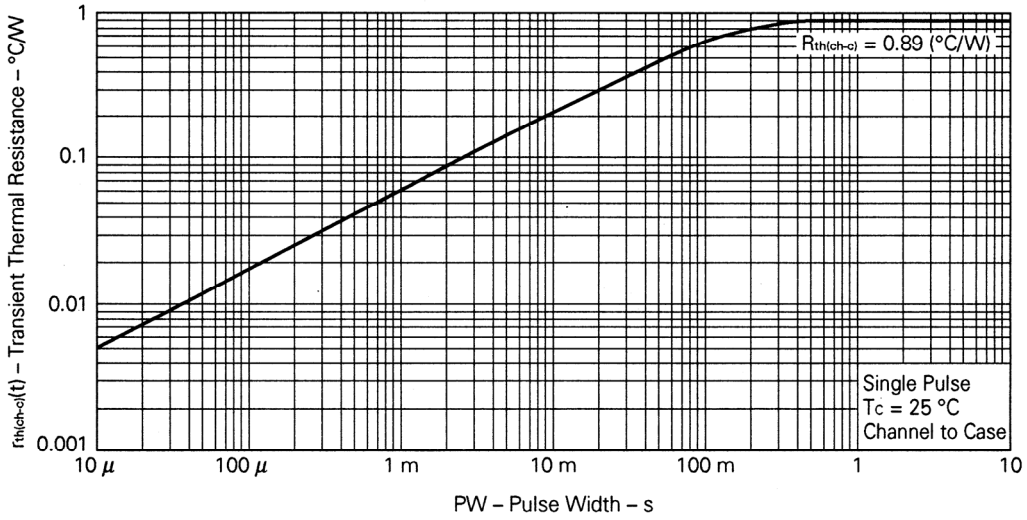
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



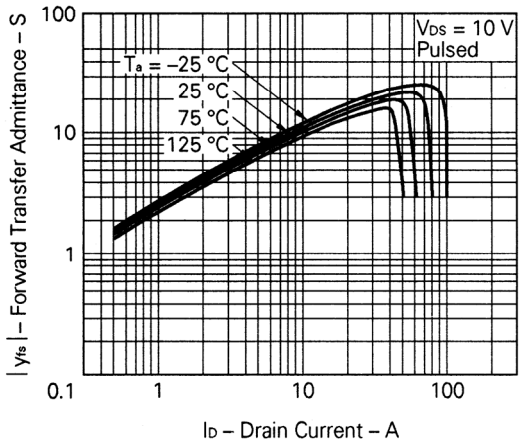
TRANSFER CHARACTERISTICS



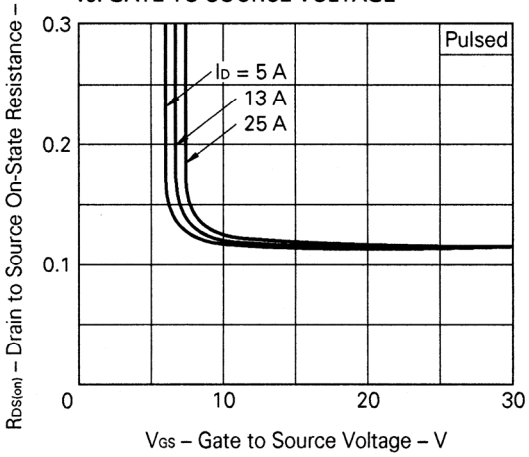
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



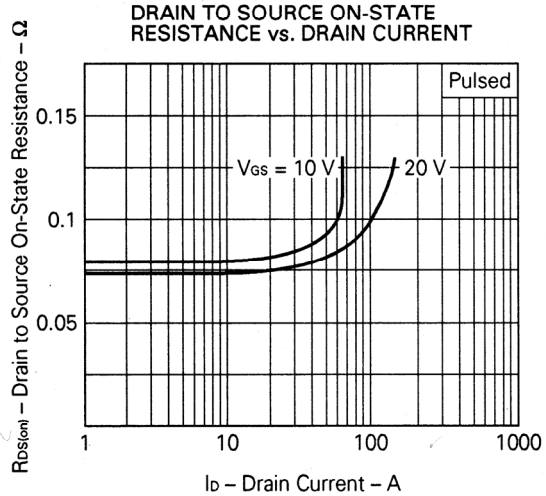
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



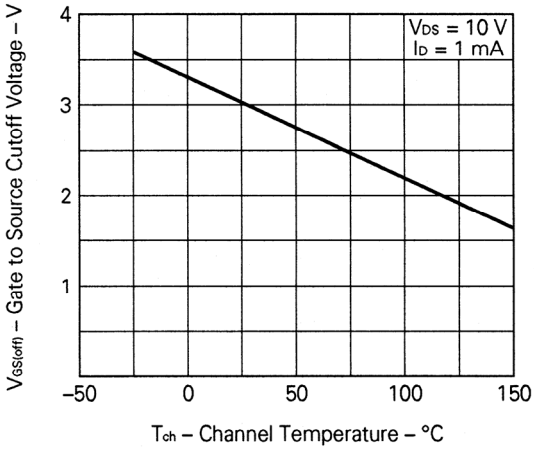
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



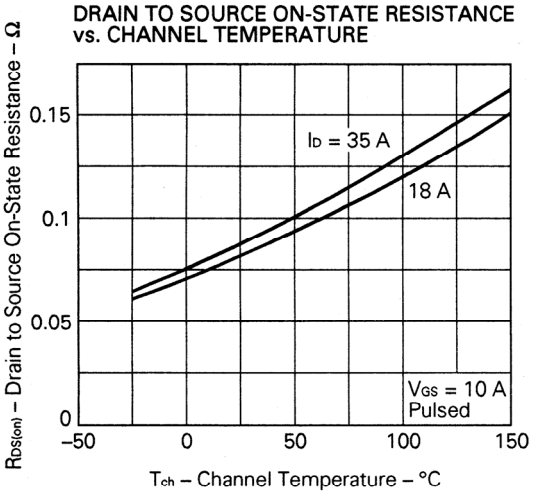
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



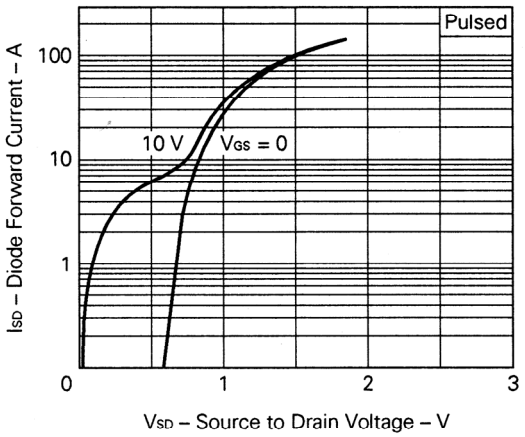
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



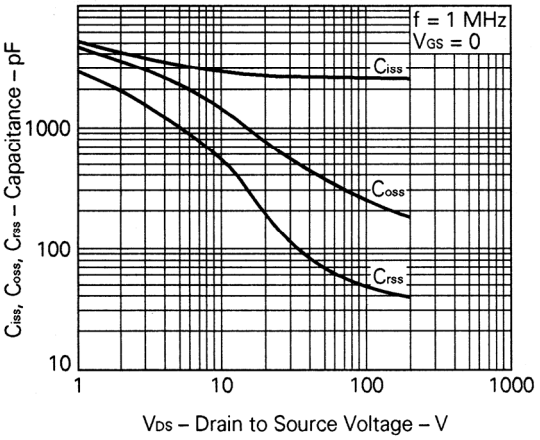
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



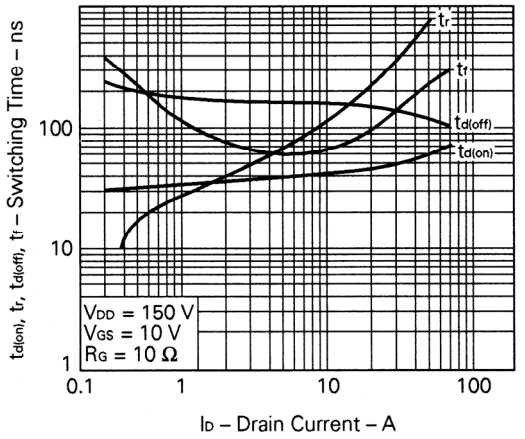
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



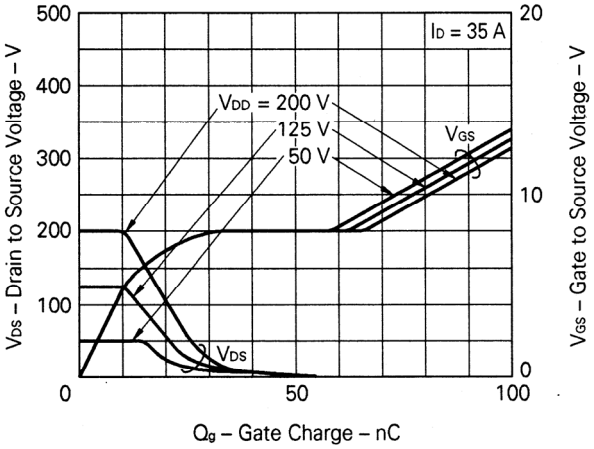
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



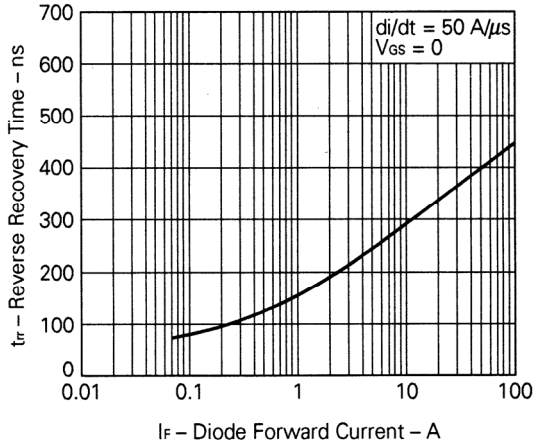
SWITCHING CHARACTERISTICS



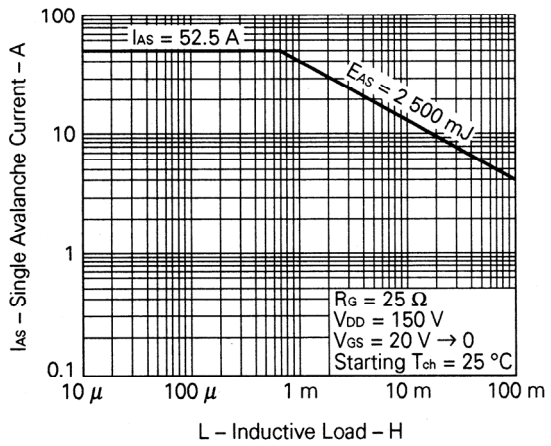
DYNAMIC INPUT CHARACTERISTICS



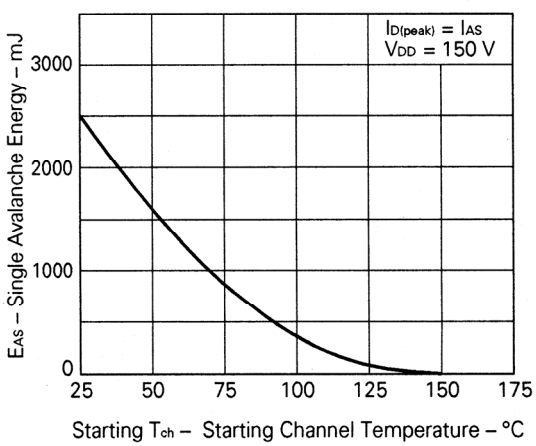
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

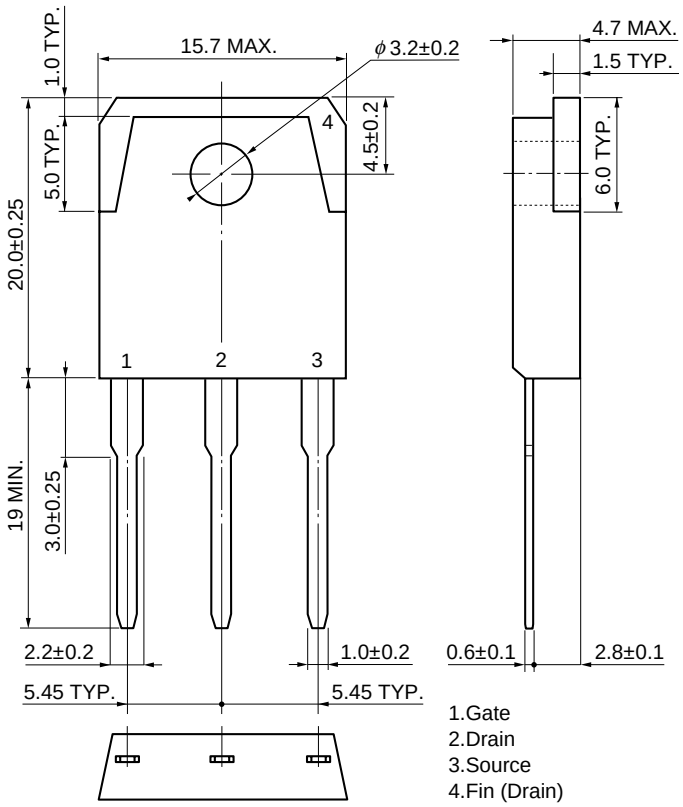


SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE

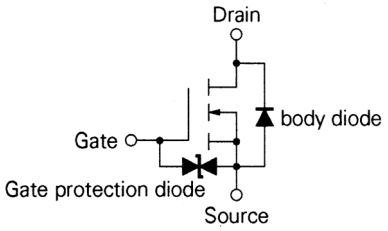


PACKAGE DRAWING (Unit: mm)

<R> **TO-3P (MP-88)**



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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