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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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2SK1334

Silicon N Channel MOS FET

REJ03G0932-0200
(Previous: ADE-208-1271)
Rev.2.00
Sep 07, 2005

Application

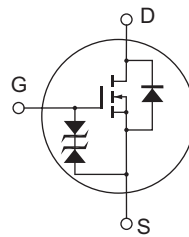
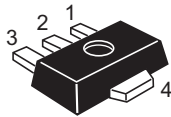
High speed power switching

Features

- Low on-resistance
- High speed switching
- Low drive current
- No secondary Breakdown
- Suitable for switching regulator and DC-DC converter

Outline

RENESAS Package code: PLZZ0004CA-A
(Package name: UPAK[®])



1. Gate
2. Drain
3. Source
4. Drain

Note: Marking is "BY".

*UPAK is a trademark of Renesas Technology Corp.

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	200	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	1	A
Drain peak current	I _{D(pulse)} ^{*1}	2	A
Body to drain diode reverse drain current	I _{DR}	1	A
Channel dissipation	P _{ch} ^{*2}	1	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. When using the alumina ceramic board (12.5 × 20 × 0.7 mm)

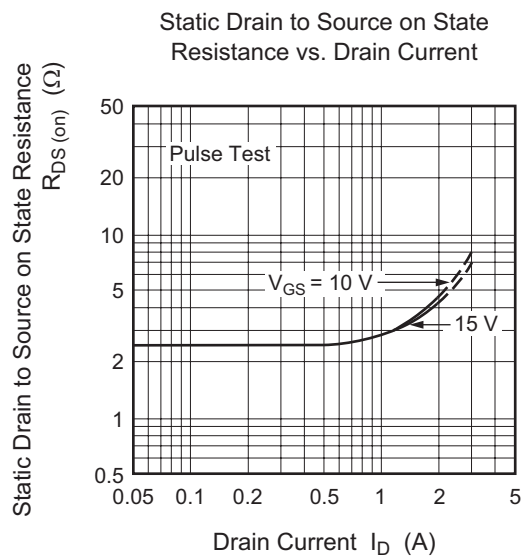
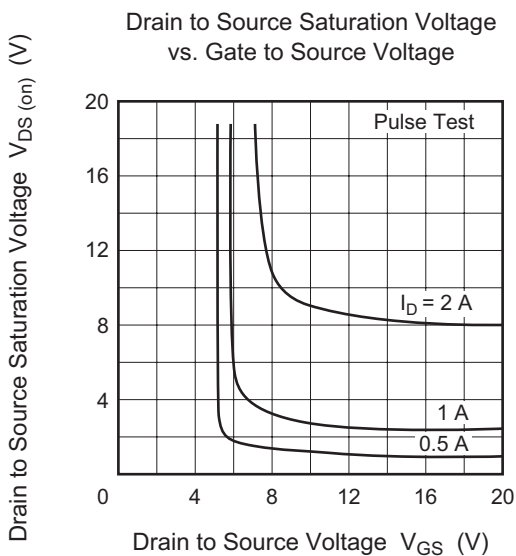
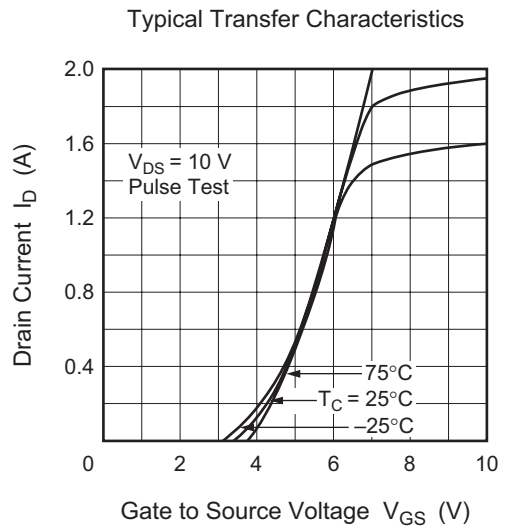
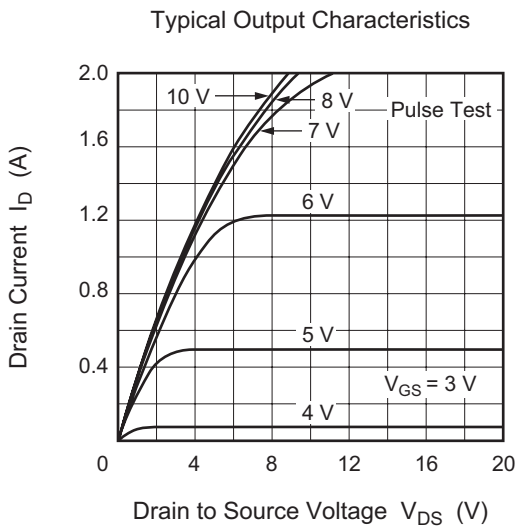
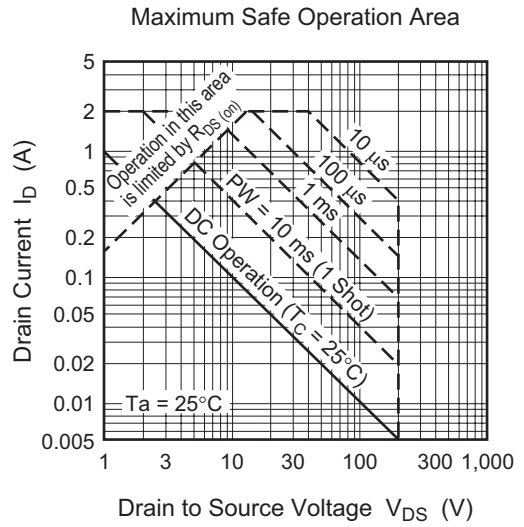
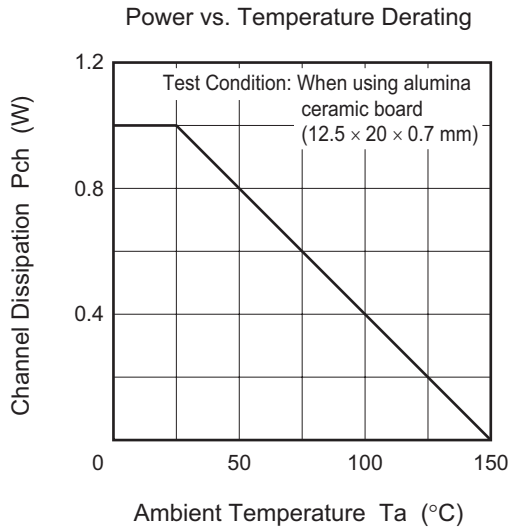
Electrical Characteristics

(Ta = 25°C)

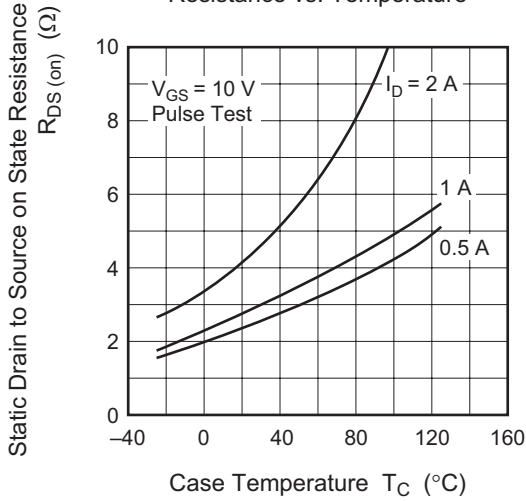
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	V _{(BR)DSS}	200	—	—	V	I _D = 10 mA, V _{GS} = 0
Gate to source breakdown voltage	V _{(BR)GSS}	±20	—	—	V	I _G = ±100 μA, V _{DS} = 0
Gate to source leak current	I _{GSS}	—	—	±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	50	μA	V _{DS} = 160 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS(off)}	2.0	—	4.0	V	I _D = 1 mA, V _{DS} = 10 V
Static drain to source on state resistance	R _{DS(on)}	—	2.5	3.8	Ω	I _D = 0.5 A, V _{GS} = 10 V ^{*3}
		—	4.5	7.0	Ω	I _D = 2 A, V _{GS} = 10 V ^{*3}
Forward transfer admittance	y _{fs}	0.4	0.6	—	S	I _D = 0.5 A, V _{DS} = 10 V ^{*3}
Input capacitance	C _{iss}	—	80	—	pF	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz
Output capacitance	C _{oss}	—	40	—	pF	
Reverse transfer capacitance	C _{rss}	—	7	—	pF	
Turn-on delay time	t _{d(on)}	—	5	—	ns	I _D = 0.5 A, V _{GS} = 10 V, R _L = 60 Ω
Rise time	t _r	—	8	—	ns	
Turn-off delay time	t _{d(off)}	—	10	—	ns	
Fall time	t _f	—	7	—	ns	
Body to drain diode forward voltage	V _{DF}	—	1.0	—	V	I _F = 1 A, V _{GS} = 0
Body to drain diode reverse recovery time	t _{rr}	—	75	—	ns	I _F = 1 A, V _{GS} = 0, di _F /dt = 50 A/μs

Notes: 3. Pulse test

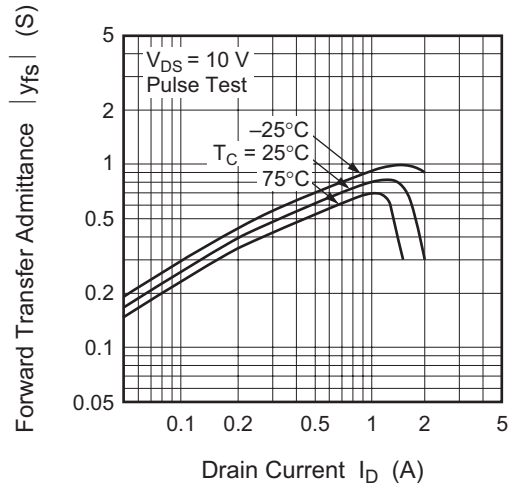
Main Characteristics



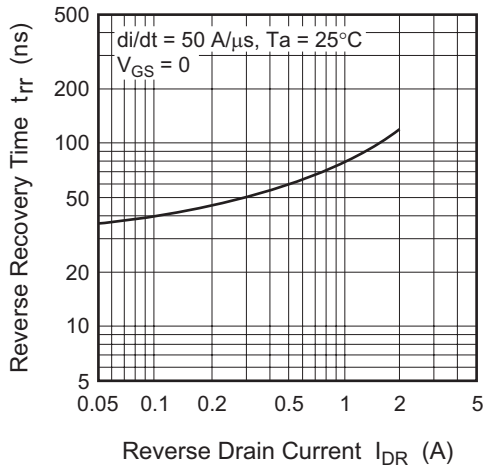
Static Drain to Source on State Resistance vs. Temperature



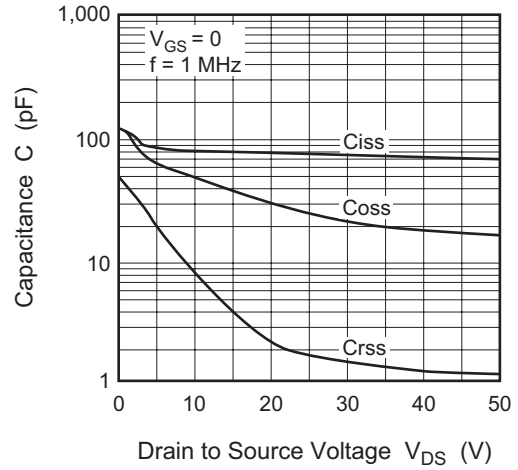
Forward Transfer Admittance vs. Drain Current



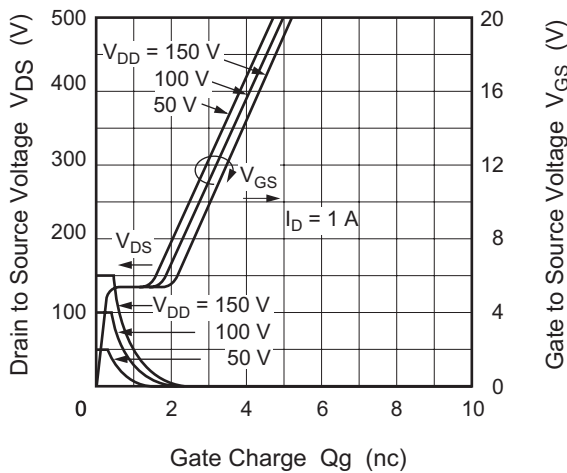
Reverse Recovery Time vs. Reverse Drain Current



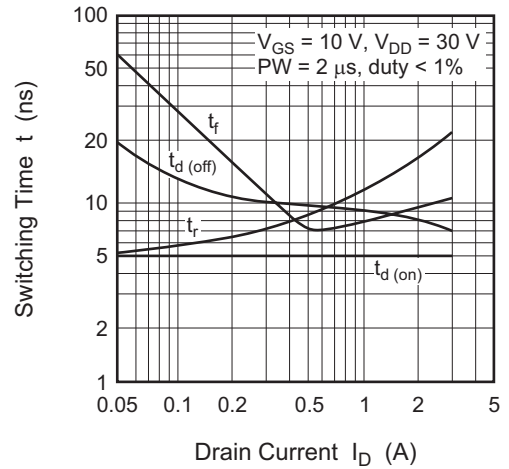
Typical Capacitance vs. Drain to Source Voltage

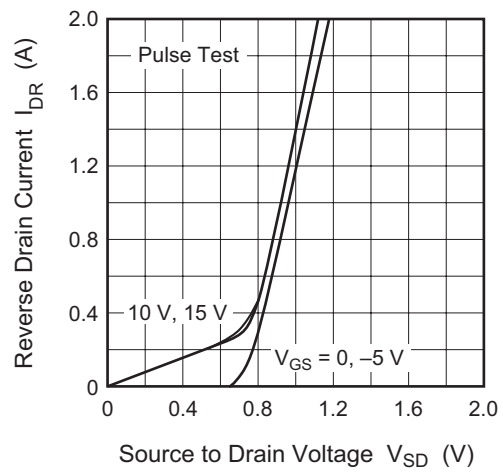


Dynamic Input Characteristics

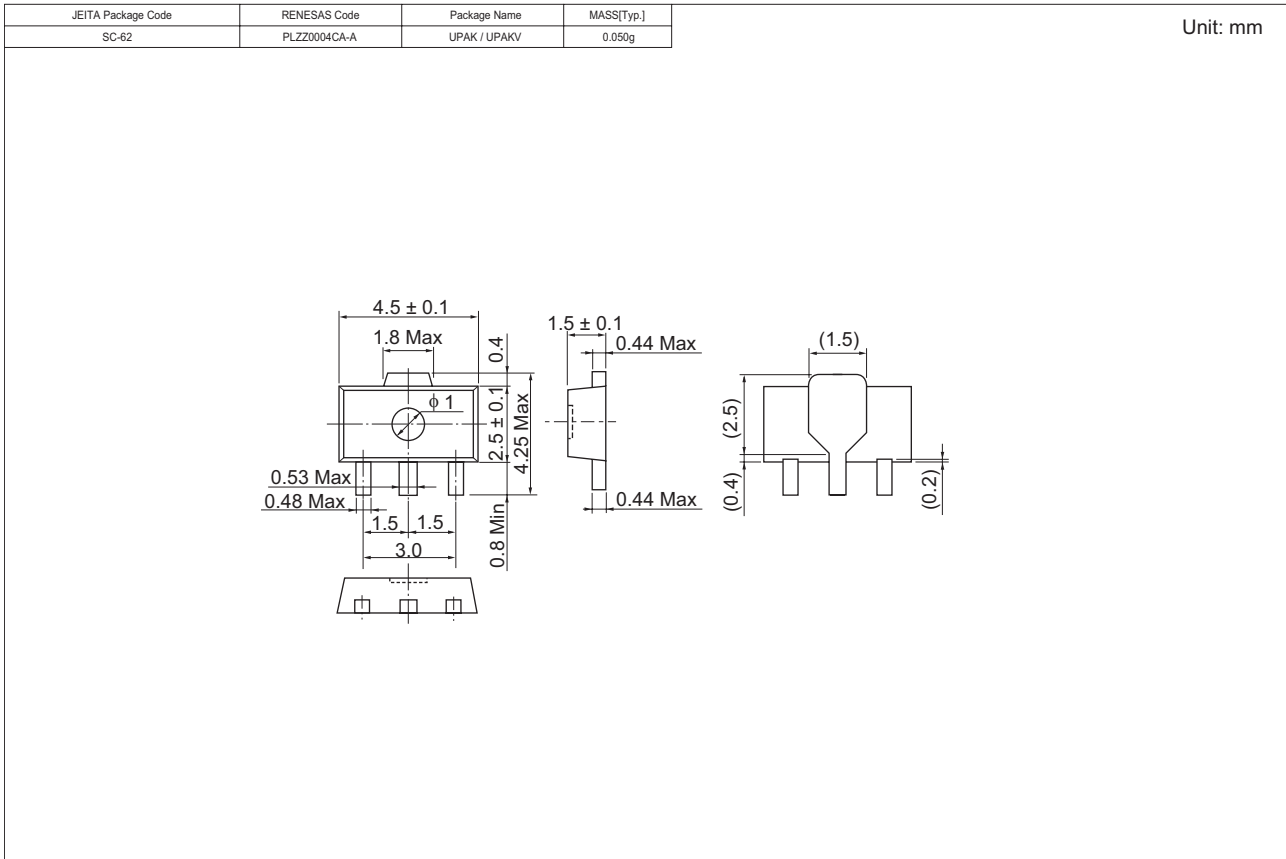


Switching Characteristics



Reverse Drain Current vs.
Source to Drain Voltage

Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
2SK1334BYTL-E	1000 pcs	$\phi 178$ mm Real, 12 mm Emboss taping

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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